Honeywell

SERIES 16

H316
CIRCUIT MODULES AND PARTS INSTRUCTION MANUAL

Doc. No. 70130072166AV Order No. FT09

Honeywell

SERIES 16

H316
CIRCUIT MODULES AND PARTS INSTRUCTION MANUAL

Doc. No. 70130072166AV Order No. FT09

November 1974

REVISION HISTORY

New Revision Level of Manual	Change No.	Effective Date	Number and New Revision Level of Affected Drawings	Pages Affected by Revision
B	7690	Jan. 1970		vi, ix, 2-20, 2-22, 2-23, 2-45, 2-47, 2-57, 2-58, 3-20, 3-21
C	7759	Feb. 1970		1-67
D	8006	Mar. 1970		1-67
E	8128	June 1970		1-21, 1-23, 1-25, 1-27, 1-29, 1-31, 1-33, 1-35, 1-37
F	8356	June 1970	70022835E 70022836E 70022841C	iv, vi, ix 2-31 2-33 2-45 2-47, 2-61, 2-62
G	8451	July 1970		2-2
H	8684	Sept. 1970		Title page (deleted), vii, viii, x, xi, xii (added); 4-4, 4-8, 4-9, 4-13, 4-23, 4-24, 4-27 — 4-31, 4-32 (deleted); 5-1 — 5-31 (added)

Publications Department, Field Engineering Division, Newton, MA 02161

Printed in the United States of America

REVISION HISTORY (Cont)

New Revision Level of Manual	Change No.	Effective Date	Number and New Revision Level of Affected Drawings	Pages Affected by Revision
J	8704	Nov. 1970	A70022955D	2-58
			P70022955E	2-58
			B70022955E	2-59, 2-60
				vi, x, xi, xii, 2-47, 2-57 — 2-59; 2-60 (added)
			P70022970B	2-61
			A70022970B	2-62
K	9313	Mar. 1971		1-49, 1-50, 1-51, 1-53
L	9375	Apr. 1971		2-49, 2-64
M	9423A	May 1971		2-1, 2-4, 2-5, 2-10, 2-13 — 2-28, 4-19, 5-9
			C70022843D	2-29
			C70022835F	2-31
			C70022836F	2-33
			C70022837B	2-35
			C70022838C	2-37
			C70022839E	2-39
			C70022840B	2-41
			C70022841C	2-45
			P70022841C	2-47
N	9529A	June 1971		3-19, 3-21
P	9650	July 1971	C70022839E	2-39
Q	9689	July 1971		1-1, 1-19, 1-97 — 1-103, 3-1 — 3-44
R	9919	Nov. 1971		1-49
			C70023327C	1-50
			C70023697C	1-51, 1-53
S	10140	Jan. 1972		2-60
T	10189	Feb. 1972		vi thru x; xi, xii added; 4-1 thru 4-31; 4-33 thru 4-77 added; 5-1 thru 5-30; 5-31 thru 5-49 added
U	10218	Mar. 1972		2-52
V	10260	Apr. 1972		v, 2-49, 2-63 thru 2-66; 2-67 thru 2-73 added
			C70022838D	2-37
			70022841D	2-45, 2-47
W	10229	Apr. 1972	70023412H	3-9, 3-10
Y	20049	June 1972		1-61
			70023329E	1-62
			70023990B	1-63

REVISION HISTORY (Cont)

New Revision Level of Manual	Change No.	Effective Date	Number and New Revision Level of Affected Drawings	Pages Affected by Revision
Z	20593	Sept. 1972	--	1-49, 1-51, 1-53, 1-61, 1-67, 3-35
AA	20707	Oct. 1972	--	4-1, 4-48, 4-65, 4-68, 4-71, 4-72, 4-79 (added)
AB	20085	Dec. 1972	--	4-13
AC	20328	Jan. 1973	--	1-33
AD	30090	March 1973	--	4-68, 4-79
AE	30110	April 1973	--	1-19, 1-73 thru 1-76, 1-77, 1-79, 2-5 2-27, 2-43 (deleted), 3-31 thru 3-33
AF	30136	May 1973	--	3-36, 3-38, 3-39,
			A70032670C	3-44
AG	31471	Aug. 1973	C70025464C	1-97 thru 1-99 (added)
			C70025966B	1-101 thru 1-103 (added)
			--	CSM-150 Core Memory Module, 3-1 thru 3-62 (added)
				Chapters IV and V (deleted)*
AH	30795	Sept. 1973	C70032889B	3-49
			C70032890C	3-31
			C70032891B	3-33
			C70032892B	3-35
			C70032893B	3-37
			C70032894B	3-39
			C70032895B	3-41
			C70032896B	3-45
			C70032897B	3-43
			C70032899B	3-47
			C70050524B	3-56
AJ	30216	Sept. 1973	70023412N (Sheets 1 thru 8)	4-3 thru 4-10
			70023412N (Sheet 9)	4-11 (added)
AK	31273	Oct. 1973	C70032890C	3-31
			D70033040B	3-59
AL	30996	Nov. 1973	C70032895C	3-41
			C70032896C	3-45
AM	32132	Jan. 1974	--	Addendum added
AN	30222	Feb. 1974	D70031961G	Included in Rev. AM
			D70031976D	

*Information contained in Chapters IV and V now appears in Document Number 70130072759, Order Number M-1532.

REVISION HISTORY (Cont.)

New Revision Level of Manual	Change No.	Effective Date	Number and New Revision Level of Affected Drawings	Pages Affected by Revision
AP	40230	July 1974	D70030064Z	3-63 through 3-66 added
			D70023412P	4-3 through 4-11
AR	40524	July 1974	D70033040C	3-59
AS	40658	Aug. 1974		A-5, A-7
AT	40785	Sept. 1974	P70050523C	3-53
AU	40860	Sept. 1974		1-41
AV	41059	Sept. 1974		3-57, 3-58

CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

CONTENTS (Cont)

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

ILLUSTRATIONS (Cont)

TABLES

PREFACE

This instruction manual provides complete descriptive and reference material for the circuit modules and parts used in the H316 General Purpose Computer manufactured by Honeywell Inc., Framingham, Massachusetts. Three types of H316 computers are manufactured: Types 316-01, 316-0100, and 316-0110. The differences among the three are, for the most part, mechanical and, unless specifically stated, the parts for the three are the same. Options are documented in separate manuals.

This manual is divided into four chapters: Chapter I contains technical specifications, microcircuit characteristics, and individual assembly illustrations and parts listings for the logic modules. Chapters II and III provide instructions for proper operation and maintenance of the CSM-160 and CSM-150 core memories, respectively, and associated PAC logic modules. A detailed illustrated parts breakdown is presented in Chapter IV as an aid to service personnel in identification and procurement of replaceable parts including assemblies and components.

CHAPTER 1
PLUG-IN CIRCUIT MODULES

This chapter contains specifications for integrated circuit plug-in devices used throughout the H316 General Purpose Computer. Section 1 contains the information pertinent to integrated circuit characteristics associated with the logic module subassemblies. Section 2 contains detailed assembly and schematic drawings and parts listings for each logic circuit module type.

SECTION 1
INTEGRATED CIRCUIT CHARACTERISTICS

This section contains general specifications and detailed technical data for the integrated circuits used on the H316 logic modules.

SPECIFICATIONS

All performance specifications are guaranteed based on worst-case tolerances. Actual performance will invariably exceed these specifications. The following specifications apply to all circuit types.

Input Switching Thresholds

The following definitions apply to all electronic signals. A "passive" signal is defined as a signal that denotes voltage potential between +2.5 volts and $+V_{cc}$. An "active" signal is defined as a signal that denotes potential between 0 volt and +0.95 volts. Figure 1-1-1 defines the switching thresholds of the circuits. An "active" input applied to a gate will guarantee a "passive" output. If a "passive" signal is simultaneously applied to all inputs of a NAND gate, the output is guaranteed to be "active."

Output Logic Levels (for all circuit types)

Active Levels: 0 to 0.5 volts
Passive Levels: 3.5 to 6.3 volts

Temperature Range

Operating (case temperature): 0°C to +80°C
Storage: -65°C to +150°C

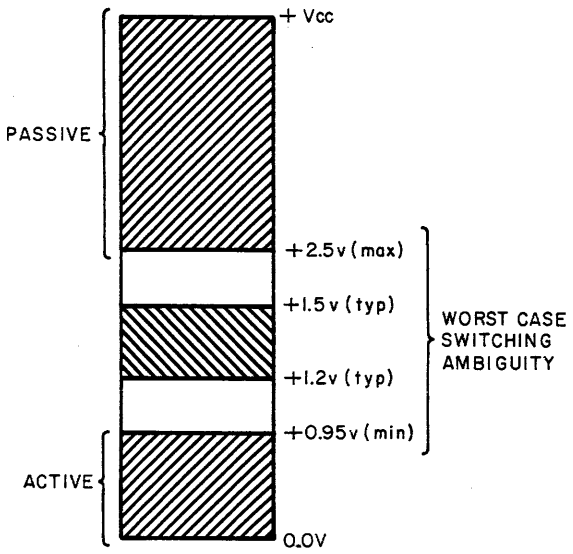


Figure 1-1-1. Switching Thresholds

Power Supply Requirements

Nominal:	+5.5V to +6.0V
Operating Range:	+5.1 to +6.3V
Absolute Maximum Rating:	+8.0V

Fan-In Expansion Using Nodes

Many of the integrated circuits have expansion nodes available on gate inputs allowing input gating expansion by connecting discrete diodes. As many as twenty silicon diodes may be connected to one node without degrading dc performance. However, there is degradation in the turn-on delay as the stray capacitance on the node point is increased. This delay increase amounts to 1.5 nanoseconds per picofarad of added capacitance.

Loading

Loading and drive specifications are expressed in terms of current (milliamperes). Input load current is the amount of current that the driving source must sink when the source is active. A passive drive source is not required to sink or supply current except for minor amounts of leakage.

Basic NAND Circuit

All NAND gates are ground-emitter, inverter amplifiers. All inputs are diode-buffered, and the output is the voltage of a saturated transistor when it is in the active state. The following circuits have an internal resistor to V_{cc} connected to the collector

of each output: 930, 961, 946, 949, 936, 937, 962, 963, and F-19 (excluding circuit C). The F-04 flip-flops also have resistors to V_{cc}. The following contain total pole circuits which provide a low drive impedance when the circuits go from the active to passive state: F-03, F-09, 932, F-19 (circuit C only). The following circuits have open collectors: F-01, 944, and 032. All outputs are protected so that accidental grounding of an output will not cause circuit damage.

When all inputs to a NAND gate have passive signals applied, the output will be active. If any one input to a NAND gate is active, the output will be passive.

TYPE F-01 NAND GATE (CCD 70 950 100 001)

The F-01 dual NAND gate (Figure 1-1-2) has two 3-input gates, each with an input node and a separate kilohm load resistor which is connected to $+V_{cc}$.

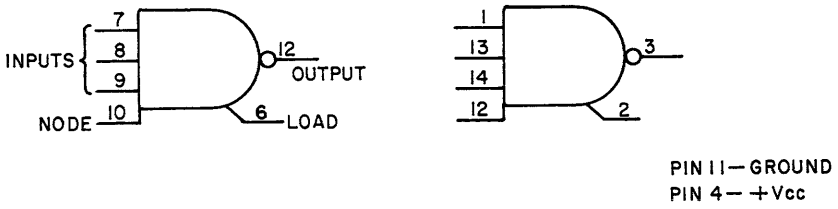


Figure 1-1-2. F-01 Dual NAND Gate

Specifications

Input Loading:	2.0 mA
Output Drive:	23.0 mA
Circuit Delay:	30 ns (max) measured at 1.5V level with 75 pF stray capacitance

TYPE F-03 POWER AMPLIFIER (CCD 70 950 100 003)

The F-03 power amplifier microcircuit (Figure 1-1-3) has two 3-input inverter amplifiers with nodes for input gating expansion. The power amplifier circuit is logically equivalent to the F-01 gate but has twice the dc drive and three times the ac drive capability.

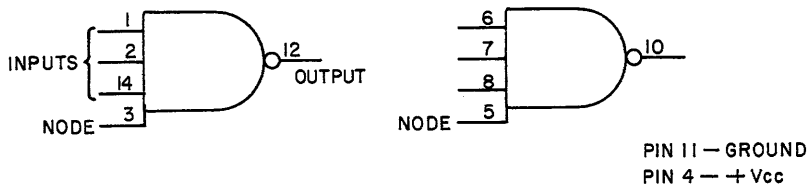


Figure 1-1-3. F-03 Power Amplifier

Specifications

Input Loading: 4.0 mA

Output Drive: 50.0 mA

Circuit Delay: 30 ns (max) measured at 1.5V level with 250 pF stray capacitance

TYPE F-04 FLIP-FLOP (CCD 70 950 100 004)

The standard μ-PAC integrated circuit flip-flop, type F-04, is a double-rank, J-K flip-flop with dc set and reset capability. Figure 1-1-4 shows the logic symbol and equivalent logic circuit.

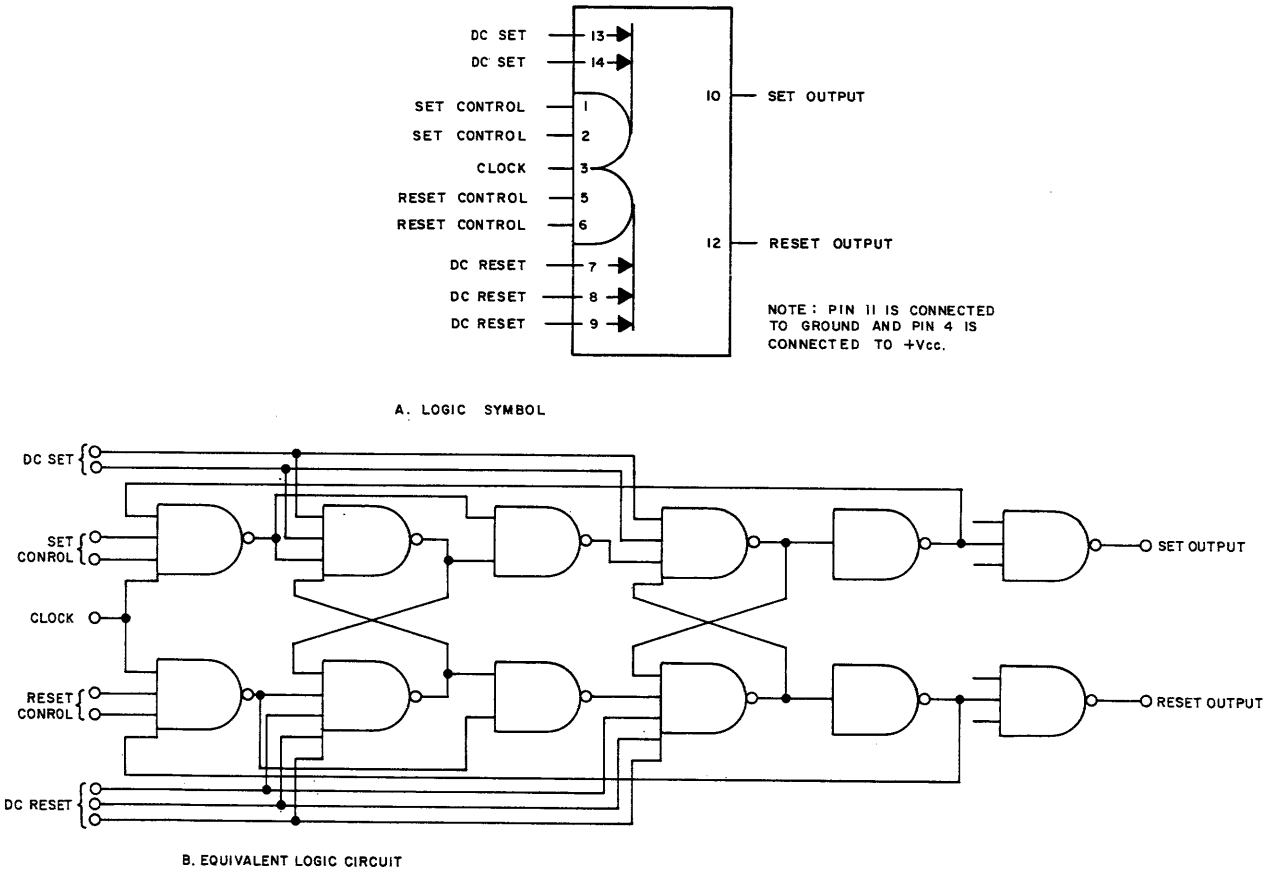


Figure 1-1-4. Type F-04 Flip-Flop Logic Symbol and Equivalent Logic Circuit

The clock gate portion of the flip-flop is composed of the clock and the set and reset control inputs. The control inputs are energized by passive signals. A positive pulse on the clock will cause the flip-flop to assume the state determined by the condition of the control inputs. With J-K circuitry, no combination of the control input signals can cause an ambiguous state.

The set and reset control inputs may be used as follows.

a. To gate clock pulses
b. As direct set and reset inputs
c. As another clock input when a set and a reset control are tied together.

For dc operation, voltage levels are used on the dc inputs. Signals applied to the dc set and reset inputs take precedence over any ac gating. However, output spikes may occur when the reset clock gate is activated during a dc set, or vice-versa. Such spikes can be eliminated by tying the dc set input to a reset control input and tying the dc reset input to a set control input.

Pulse Dodging

The flip-flop utilizes the double-rank technique of pulse dodging (Figure 1-1-5). When the clock input makes the positive transition, the state of the input flip-flop is fixed and data transfer from the input flip-flop to the input of the output flip-flop is inhibited. On the negative transition of the clock input, data from the input flip-flop is shifted to the output flip-flop and the inputs to the input flip-flop are inhibited. Thus the clock provides intrinsic pulse dodging by means of trailing edge triggering. This feature permits strobing of the flip-flop output with input triggering signals.

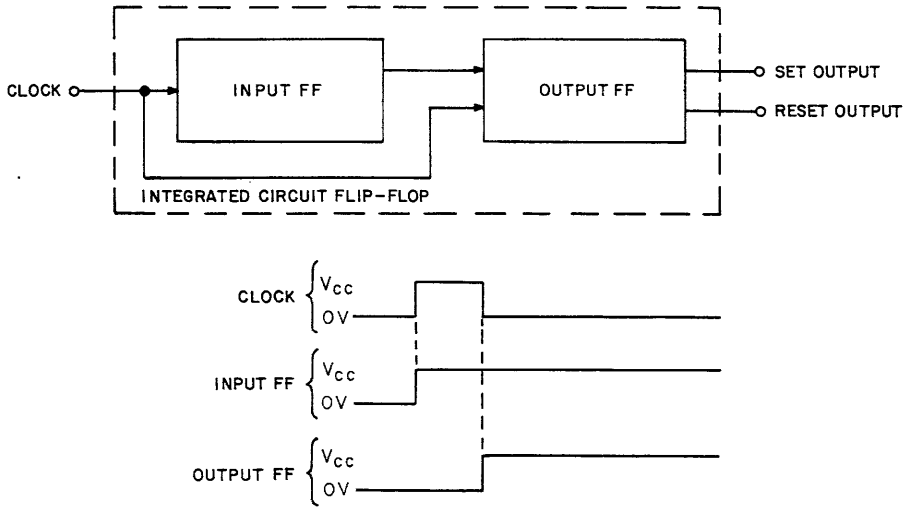
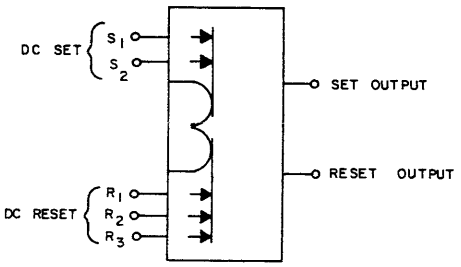


Figure 1-1-5. Double-Rank Flip-Flop Pulse Dodging, Timing Diagram

DC Operation

If either dc set goes to ground, the flip-flop will assume the set state; if any dc reset goes to ground, the flip-flop will assume the reset state. If both a dc set and a dc reset go to ground at the same time, both the set and the reset outputs will be ambiguous. Figure 1-1-6 contains diagrams and equations describing this mode of flip-flop operation.

A) LOGIC DIAGRAM



B) Truth Table and Boolean Equations

S_D - AND result of the dc set inputs. $S_D = S_1 \cdot S_2$

R_D - AND result of the dc reset inputs. $R_D = R_1 \cdot R_2 \cdot R_3$

F - state of the flip-flop (set output)

F' - previous state of the flip-flop

S_D	R_D	F
0V	0V	(Condition not allowed. Output will be ambiguous.)
0V	V_{cc}	Set
V_{cc}	0V	Reset
V_{cc}	V_{cc}	F' (no change) $F = R_D (\overline{S}_D + F')$

C) TIMING DIAGRAM

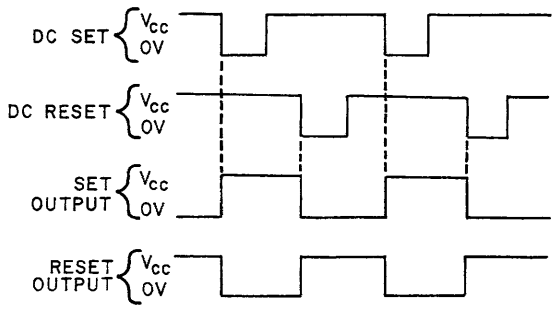
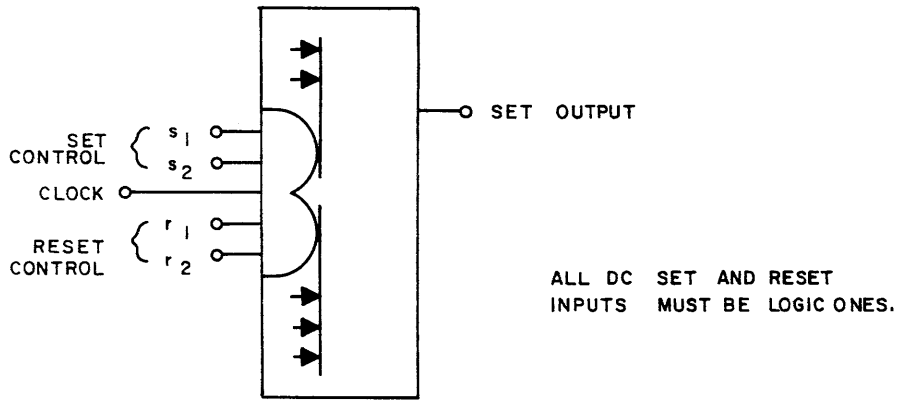


Figure 1-1-6. DC Operation

Control Inputs Used to Steer Clock Pulses

If Vcc is applied to both the set controls (S_C) and the reset controls (R_C), the flip-flop will be complemented by the application of a clock pulse. If only S_C or R_C is at Vcc, the state of the flip-flop will be a set or reset, respectively, after the clock is energized. If both S_C and R_C are at ground, the flip-flop will remain in its previous state. One restriction is that when a control input is used to gate the clock, the control input cannot make a negative transition while the clock is a ONE. Figure 1-1-7 contains diagrams and equations describing this mode of flip-flop operation.

A) LOGIC DIAGRAM



B) Truth Table and Boolean Equations

S_C - AND result of the set control inputs, $S_C = s_1 \cdot s_2$

R_C - AND result of the reset control inputs, $R_C = r_1 \cdot r_2$

F' - previous state of the flip-flop

F - state of the flip-flop after the clock pulse

S	R	F'	F	
0V	0V	0V	0V	NO CHANGE
0V	0V	V_{cc}	V_{cc}	
0V	V_{cc}	0V	0V	RESET
0V	V_{cc}	V_{cc}	0V	
V_{cc}	0V	0V	V_{cc}	SET
V_{cc}	0	V_{cc}	V_{cc}	
V_{cc}	V_{cc}	0V	V_{cc}	COMPLEMENT
V_{cc}	V_{cc}	V_{cc}	0V	

$$F = S_C\overline{F'} + \overline{R}_C F'$$

557

Figure 1-1-7. Control Inputs Used to Gate Clock Pulses (Sheet 1 of 2)

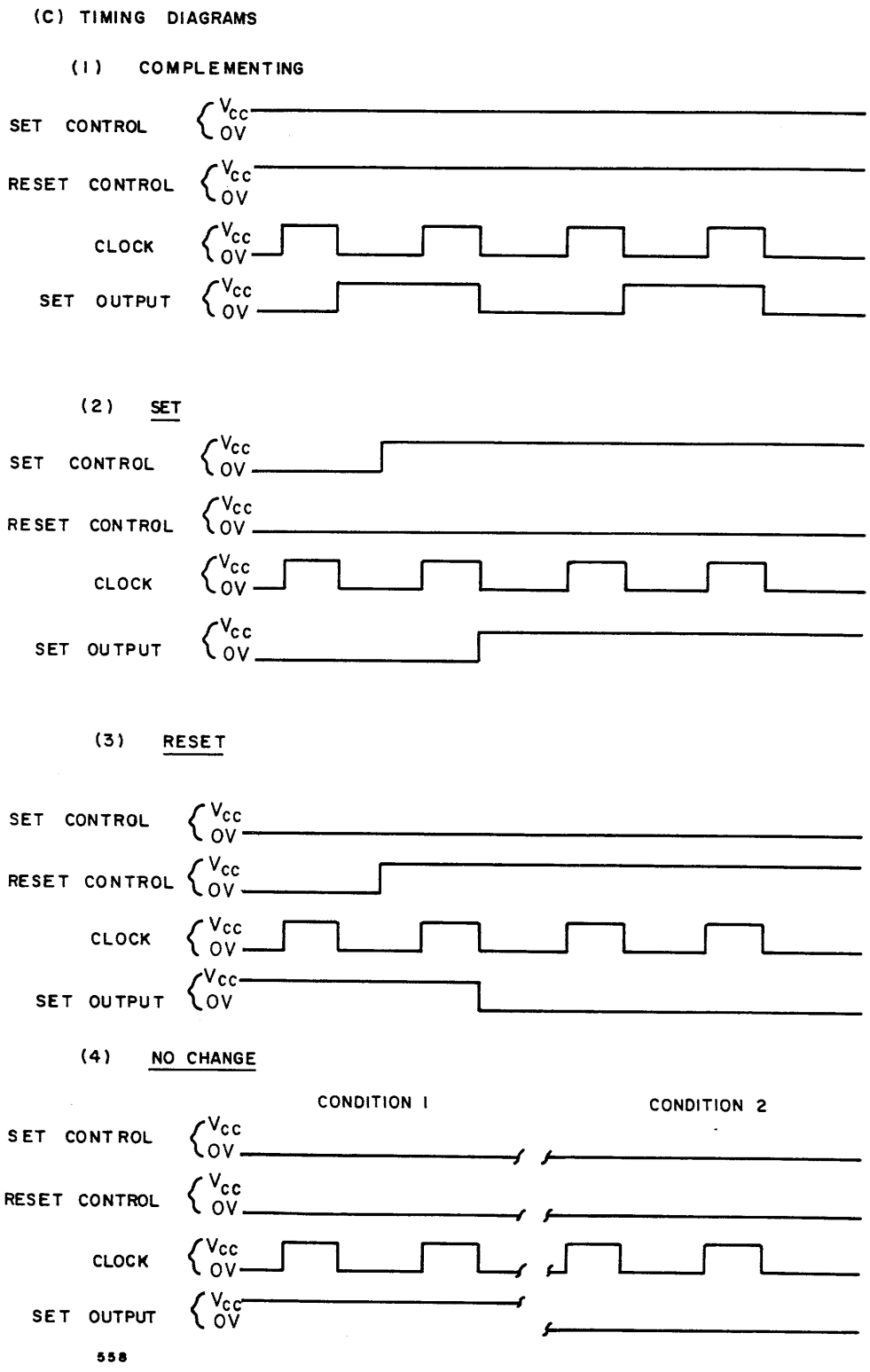


Figure 1-1-7. Control Inputs Used to Gate Clock Pulses (Sheet 2 of 2)

Control Inputs Used as a Second Clock

A set and a reset control can be tied together and used as another clock input. In this case, the resultant clock is the ANDed result of both clocks. Figure 1-1-8 contains diagrams describing this mode of flip-flop operation.

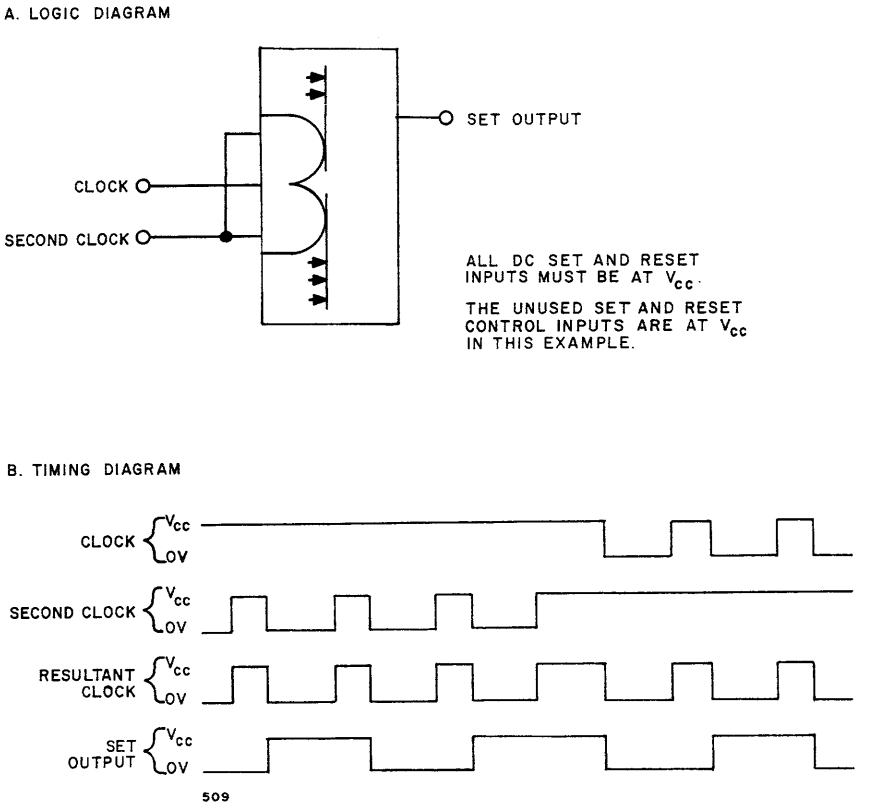
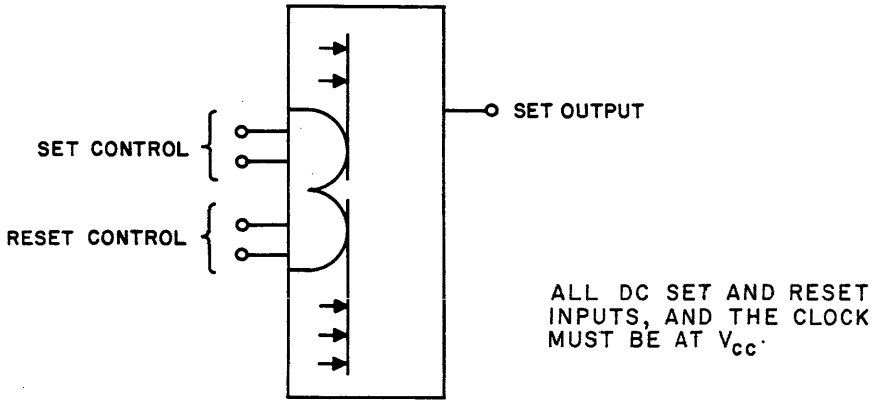


Figure 1-1-8. Control Inputs Used As a Second Clock

Control Inputs Used Directly to Set or Reset

The set and the reset control inputs can also be used separately to change the state of the flip-flop. When the clock is at V_{cc}, the first control input that goes from V_{cc} to ground acts as the clock input. After a set control changes from Vcc to ground, the flip-flop will be in the set state. After a reset control changes from Vcc to ground, the flip-flop will be in the reset state. Figure 1-1-9 contains diagrams and equations describing this mode of flip-flop operation.

A. LOGIC DIAGRAM



B) Boolean Equations

S_C - AND result of the set control inputs

R_C - AND result of the reset control inputs

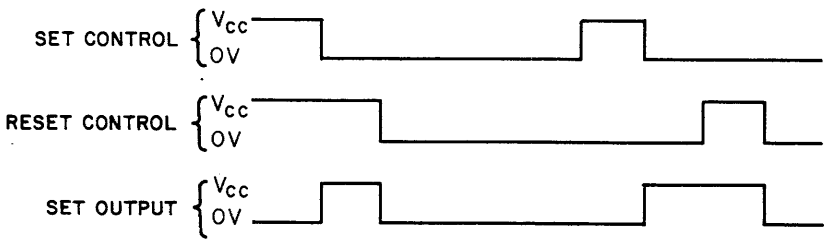
F - state of the flip-flop

primes (') - previous state of a signal

$F = S'_C \cdot \overline{S}_C$ (setting operation)

$\overline{F} = R'_C \cdot \overline{R}_C$ (resetting operation)

C. TIMING DIAGRAM



560

Figure 1-1-9. Control Inputs Used Directly to Set or Reset

Input Loading

DC inputs:	1.33	mA
Clock input:	2.0	mA
Control inputs:	2.0	mA

Output Drive Capability

8 unit loads (both outputs)
(Capable of also driving 75 pF total capacitance with delays as specified.)

Circuit Delay

The following circuit delays are specified from the +1.5V level of the input signal to the +1.5V level of the output signal.

Clock input (negative transition) to latest output	45 ns (typ) 60 ns (max)
DC set input to set output or DC reset input to reset output	65 ns (typ) 80 ns (max)
DC set input to reset output or DC reset input to set output	45 ns (typ) 60 ns (max)

Clock and Control Input Timing Requirements

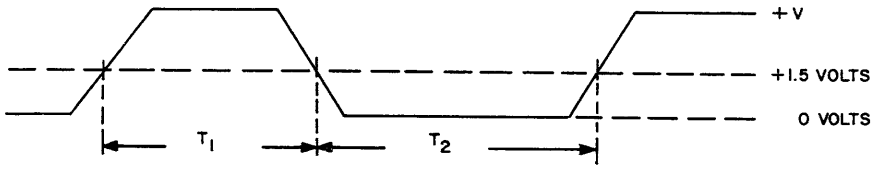
To trigger the flip-flop at the clock or control inputs, pulses must meet the requirements shown in Figure 1-1-10.

DC Input Timing Requirements

To activate a dc input, signals must meet the requirements of Figure 1-1-11.

Control Inputs

Figure 1-1-12 shows the timing requirements of the set and reset control inputs when they are being used to steer the triggering clock input to set the flip-flop. The reset control input must be completely switched to ground before the clock starts positive. No control input should go from Vcc to ground while the clock is positive. The set control input must be switched to Vcc at least 40 ns before the clock starts towards ground. The clock must be a positive pulse of 40 ns minimum duration. The flip-flop changes state on the trailing edge of the positive clock pulse. Reset timing is the same, except that the time relations and logic levels of the set and reset input must be interchanged.



T_1 (POSITIVE TIME) = 40 NS (MIN)

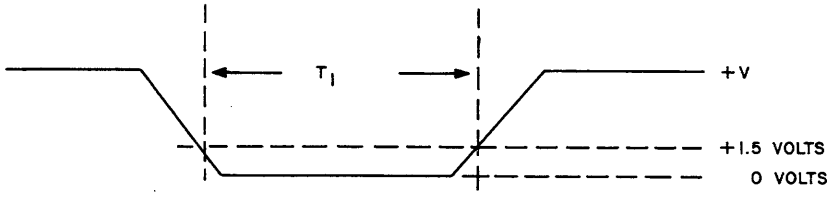
T_2 (NEGATIVE TIME) = 60 NS (MIN)

+V = +3.0 VOLTS (MIN)

T_{RISE} AND T_{FALL} REQUIREMENT – ANY μ-PAC OUTPUT SIGNAL WILL RELIABLY TRIGGER THE FLIP-FLOP.

561A

Figure 1-1-10. Flip-Flop Input Pulse Requirements

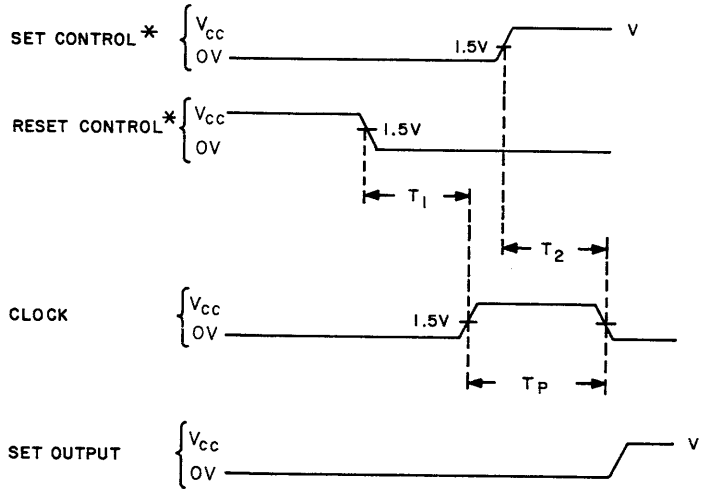


T_1 (TIME AT 0 VOLT) = 80 NS (MIN)

V = 3.0 VOLTS (MIN)

A561

Figure 1-1-11. DC Set and Reset Input Signal Requirements



*INTERCHANGE SET AND RESET CONTROL TIMING TO RESET THE FLIP-FLOP

(T_1) = 0 (MIN)

(T_2) = 40 NS (MIN)

(T_P) = 40 NS (MIN)

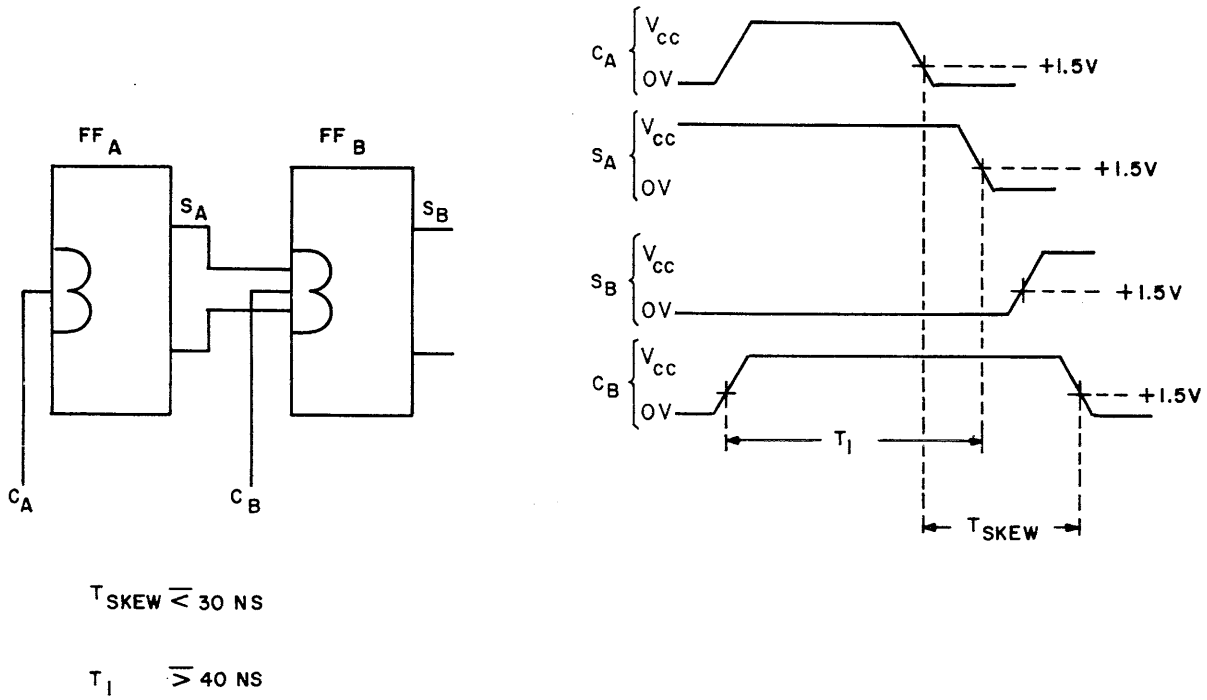
(V) = 3.0 VOLTS (MIN)

562

Figure 1-1-12. Timing Requirements for Control Inputs, Using Clock Triggering

Maximum Allowable Clock Skew

In cases where a register is being driven by clock (shift) signals from different sources, the output of one stage may arrive at the next stage before late clock signal. If the delay between the early and late clock signals is more than 30 ns, erroneous data transfer may occur. To guarantee proper operation the allowable clock skew must be as shown in Figure 1-1-13. Note that the triggering signal to flip-flop B is S_A rather than C_B. This situation is not detrimental to the operation of the shift register. Either S_A or C_B may trigger flip-flop B, depending on which occurs first.



$T_{SKEW} \leq 30$ NS

$T_I \geq 40$ NS

Figure 1-1-13. Allowable Clock Skew, Logic and Timing

TYPE F-09 POWER AMPLIFIER (CCD 70 950 100 009)

The type F-09 high speed power amplifier microcircuit has two 4-input inverter amplifiers with nodes for input gating expansion. (See Figure 1-1-14.) The power amplifier circuit is logically equivalent to the F-01 gate but has about twice the output drive capability. It has a short circuit protection network such that accidental grounding of the output will not damage the circuit.

Specifications

Input Loading:	4.0 mA
Output Drive:	50 mA
Circuit Delay:	15 ns with 70 pF of stray capacitance

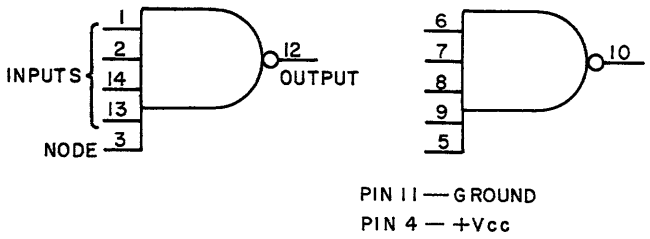


Figure 1-1-14. Type F-09 Power Amplifier Equivalent Logic Symbol

TYPE F-19 FUNCTIONAL LOGIC GATE (CCD 70 950 100 019)

The F-19 (Figure 1-1-15) has five NAND gates interconnected as a functional gating circuit. The outputs of A and B are connected together and can be used to perform the logic OR operation. This output is connected as an input to the power amplifier inverter (gate C). Gates B, D and E have input nodes (pins 2, 6 and 7) to facilitate input gate expansion by connecting discrete diodes to them.

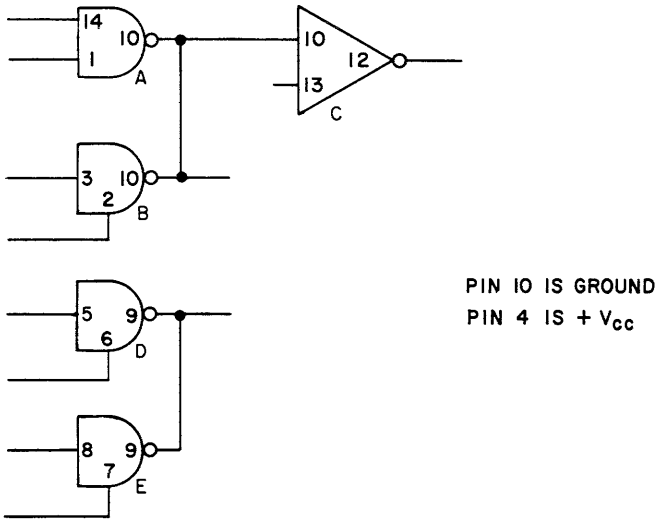


Figure 1-1-15. F-19 Logic Symbol

Specifications

Input Load:	2.0 mA
Output Drive:	Circuit A-B, D-E - 23.5 mA
	Circuit C - 40.0 mA
Circuit Delay:	20 ns per gate with 70 pF stray capacitance

TYPE 930/961 NAND GATES (CCD 70 950 105 001/009)

The 930 and 961 (Figure 1-1-16) dual 4-input NAND circuits are logically similar to the F-01 gate. The 930 has a 6 kilohm resistor connected between the output collector and $+V_{cc}$ while the 961 has a 2 kilohm resistor. Otherwise, the two are identical.

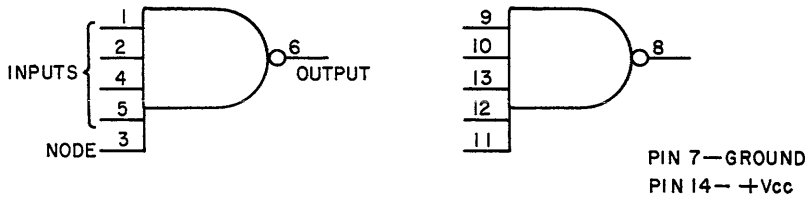


Figure 1-1-16. 930/961 Dual NAND Gates

Specifications

Input Loading:	1.6 mA	
Output Drive:	12.8 mA	
Circuit Delay:	930-75 ns	averaged over two stages
	961-50 ns	averaged over two stages

TYPE 946/949 NAND GATES (CCD 70 950 105 002/010)

The 946 and 949 (Figure 1-1-17) quad 2-input NAND circuits are similar to each other in all respects except for the value of the resistor which connects between the output collector and $+V_{cc}$. The 946 has a 6 kilohm resistor while the 949 has a 2 kilohm. The AND-OR-INVERT operation can be performed with the 6 kilohm version by connecting the output of two gates together. This can be done without substantial reduction in output drive capability.

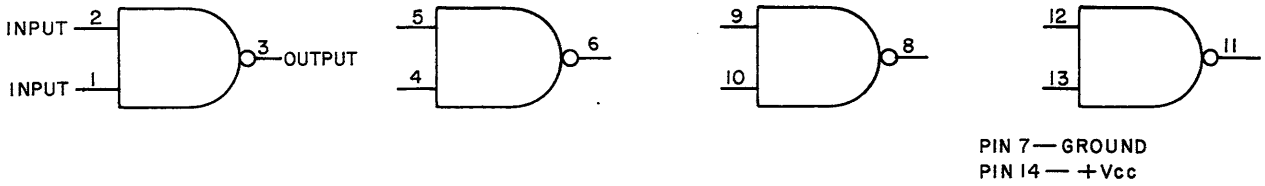


Figure 1-1-17. 946/949 Quad NAND Gates

Specifications

Input Loading:	1.6 mA	
Output Drive:	12.8 mA	
Circuit Delay:	946-75 ns	averaged over two stages
	961-50 ns	averaged over two stages

TYPE 936/937 HEX INVERTER (CCD 70 950 105 004/011)

The 936 and 937 (Figure 1-1-18) contain six inverter circuits. The 936 has a 6-kilohm resistor while the 937 has a 2 kilohm.

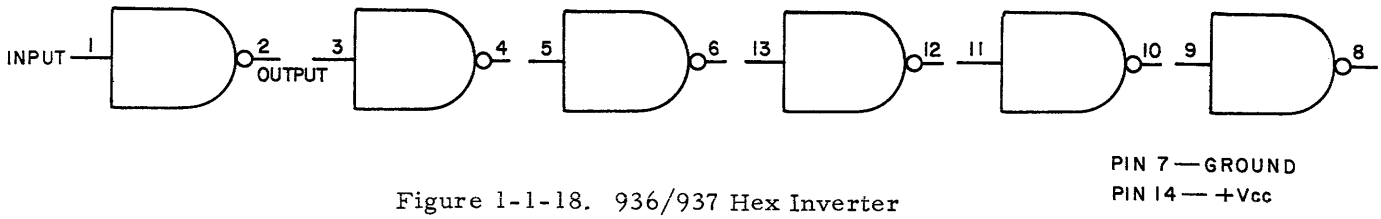


Figure 1-1-18. 936/937 Hex Inverter

Specifications

Input Load:	1.6 mA	
Output Drive:	12.8 mA	
Circuit Delay:	936-75 ns	averaged over two stages
	937-50 ns	averaged over two stages

TYPE 932 POWER AMPLIFIER (CCD 70 950 105 005)

The type 932 power amplifier has two 4-input inverter amplifiers with nodes for input gating expansion (see Figure 1-1-19). The circuit is logically equivalent to the 930 gate but has twice the output drive capability. The 932 output cannot be connected to other outputs to perform the AND-OR-INVERT logic function.

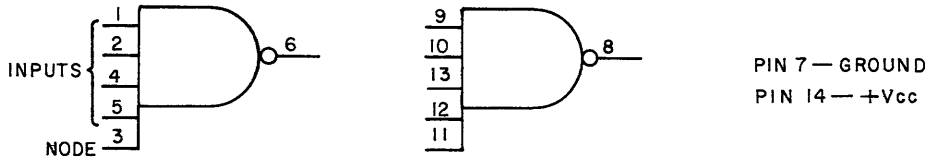


Figure 1-1-19. 932/944 Power Amplifiers

Specifications

Input Load:	1.6 mA	
Output Drive:	36.0 mA	
Circuit Delay:	80 ns	averaged over two stages driving 500 pF of stray capacitance

TYPE 944 POWER AMPLIFIER (CCD 70 950 105 008)

The 944 (Figure 1-1-19) dual 4-input power amplifier differs from the 932 only in that it has an open collector for OR operations. The turn-on delay is 40 nanoseconds when driving 120 picofarads of stray capacitance. The turn-off delay is dependent on the amount of external current that is supplied to charge the stray capacitance. The input loading and output drive specifications are similar to the 932.

TYPE 962/963 TRIP NAND GATES (CCD 70 950 105 006/012)

The 962 and 963 (Figure 1-1-20) triple 3-input NAND gates are similar to each other in all respects except for the value of resistance between the collectors and $+V_{cc}$. The 962 has a 6 kilohm resistor while the 963 has a 2 kilohm resistor.

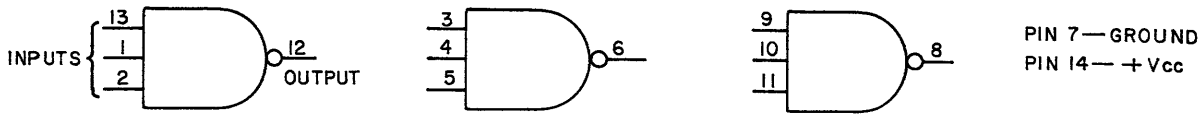


Figure 1-1-20. 962/963 Trip NAND Gates

Specifications

Input Load:	1.6 mA	
Output Drive:	12.8 mA	
Circuit Delay:	962-75 ns	averaged delay over two stages
	963-50 ns	averaged delay over two stages

TYPE 032 QUAD NAND GATE (CCD 70 950 100 032)

The 032 quad 2-input NAND gate (Figure 1-1-21) is logically similar to the 930 but it does not have a resistor between the collector and $+V_{cc}$. This feature allows many of these gates to be collector ORed without degrading the dc drive capability.

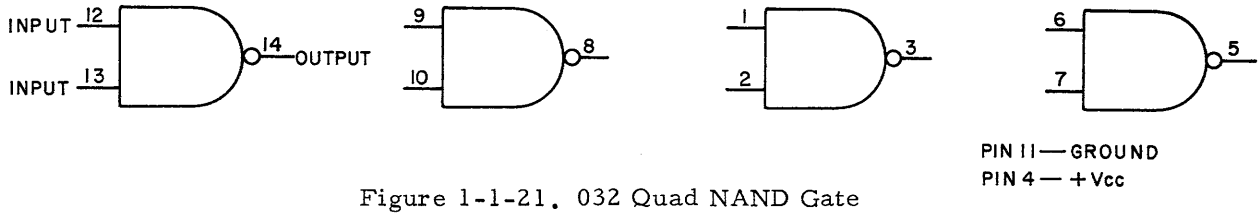


Figure 1-1-21. 032 Quad NAND Gate

Specifications

Input Load:	1.6 mA	
Output Drive:	20.0 mA	
Circuit Delay:	45 ns	averaged over two stages

SECTION 2
MODULE DESCRIPTIONS

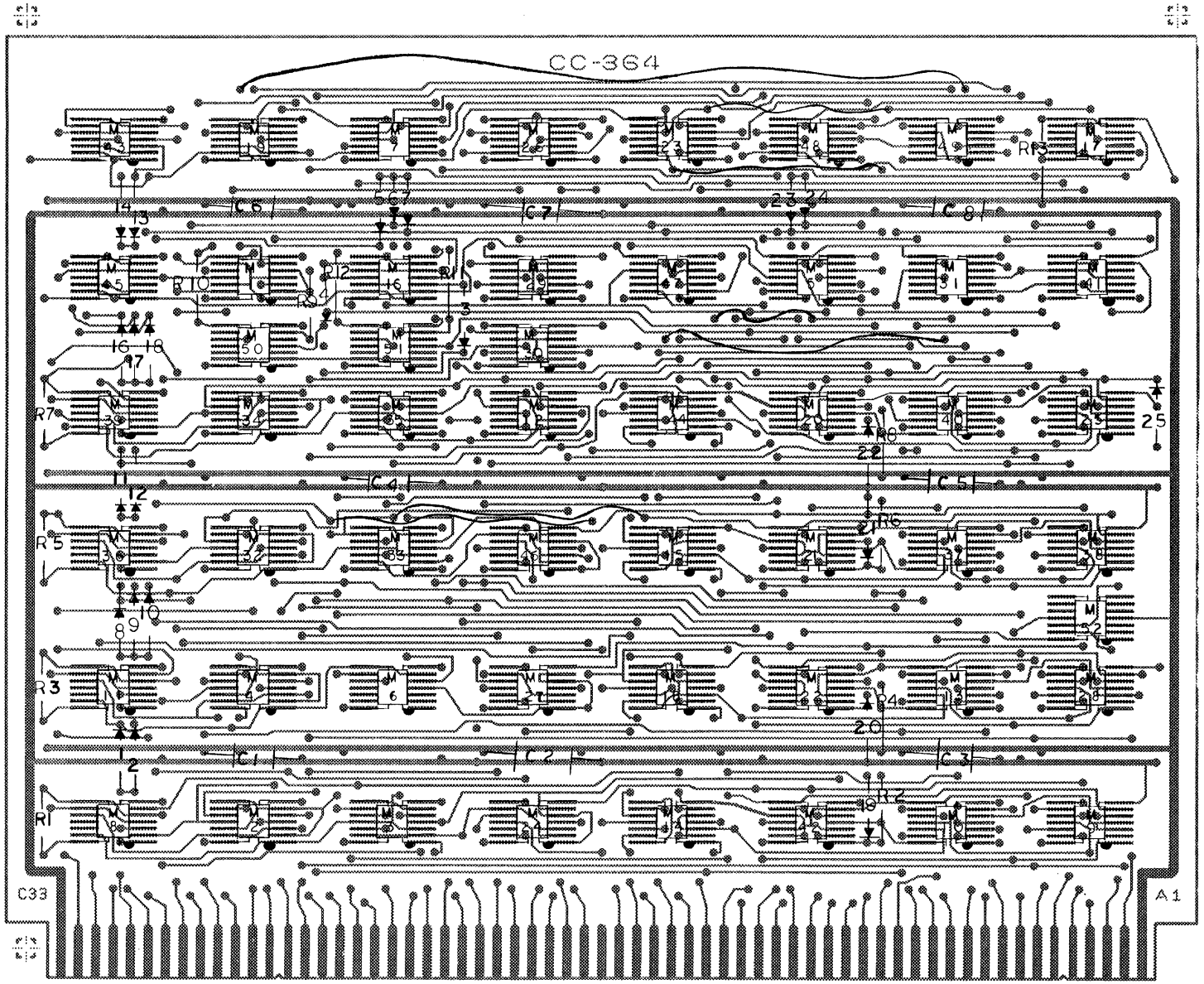
This section contains detailed assembly and schematic diagrams, and parts listings for the following logic circuit modules.

CC-364A	Columns 1-4 Module
CC-365A	Columns A-D Module
CC-366A	Columns 9-12 Module
CC-367	Address Bus Module
CC-368	Shift Register Module
CC-369B	Lamp Driver Module
CC-370	M Register Module
CC-371	Clock Module
CC-372	Regulator Counter Module
CC-373/CC-899	Memory Timing Module
CC-374	ASR Interface Module
CC-375	High Speed A-U No. 1 Module
CC-401	High Speed A-U No. 2 Module
CC-510A/CC-869	Extended Address Module
CC-558/CC-621	Memory Parity Board
CC-672	Cable PAC
CC-681	Cable PAC

COLUMNS 1-4 MODULE, MODEL CC-364A

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
CR1-CR14, CR16-CR18, CR23-CR25	DIODE: Replacement type 1N914	70 943 083 002
CR19-CR22	DIODE: Replacement type 882	70 943 024 002
M1-M4, M6 M9, M25, M28-M30, M32-M35, M38	MICROCIRCUIT: 946, quad NAND gate integrated circuit	70 950 105 002
M5	MICROCIRCUIT: 962, triple NAND gate integrated circuit	70 950 105 006
M7, M8, M11 M16, M17, M19, M31, M36, M39, M41, M43, M45, M48, M50, M51	MICROCIRCUIT: Power amplifier integrated circuit	70 950 105 008
M10, M13 M37, M40	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70 950 105 012
M12, M24, M27, M46	MICROCIRCUIT: F-01, Dual NAND gate integrated circuit	70 950 100 001
M14, M15, M18, M20-M22, M42, M44, M52	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M23, M26	MICROCIRCUIT: 936, hex inverter integrated circuit	70 950 105 004
M47, M49	MICROCIRCUIT: 930, dual NAND gate integrated circuit	70 950 105 001
R1, R3, R5, R7	RESISTOR, FIXED, COMPOSITION: 2K ±5%, 1/4W	70 932 007 056
R2, R4, R6, R8	RESISTOR, FIXED, COMPOSITION: 510 ohms ±5%, 1/4W	70 932 007 042
R9-R13	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4W	70 932 007 049



COMPONENT VIEW

Figure 1-2-1. Columns 1-4 Module Parts Location

CC-364 SHEET 1

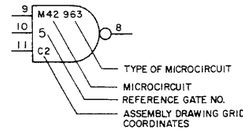
M NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6
1	B2	946	1	8	74	81		
2	B8	946	2	3	15	16		
3	C8	946	4	5	6	7		
4	B7	946	9	10	20	21		
5	F2	962	11	154	150			
6	C7	946	12	13	23			
7	C1	944	30	66				
8	A8	944	17	27				
9	H8	946	18	40	55	67		
10	G8	963	19	51	54			
11	A7	944	22	33				
12	D4	F01	130	131				
13	G7	963	24	57	60			
14	E8	032	25	38	37	38		
15	E5	032	98	108	109	110		
16	C2	944	28	29				
17	H1	944	147	148				
18	E7	032	31	43	44	45		
19	B1	944	34	35				
20	F4	032	104	118	120	121		
21	F5	032	99	111	113	114		
22	F6	032	32	46	48	49		
23	E1	936	50	56	65	71	137	143
24	D8	F01	52	53				
25	H4	946	96	119	133	145		
26	D1	936	62	68	122	128	134	140
27	D7	F01	58	59				
28	H7	946	61	73	47			
29	D2	946	63	69	135	141		
30	D3	946	64	70	136	142		
31	G2	944	14	72				
32	B5	946	75	76	88	89		
33	C5	946	77	78	79	80		
34	B4	946	82	83	93	94		
35	C4	946	84	85	86	87		
36	A5	944	90	100				
37	G5	963	92	123	126			
38	H5	946	91	112	127	139		
39	A4	944	95	105				
40	G4	963	97	129	132			
41	H2	944	138	144				
42	F8	032	26	39	41	42		
43	A1	944	101	102				
44	E4	032	103	115	116	117		
45	E5	944	106	107				
46	D5	F01	124	125				
47	E2	930	146	155				
48	F1	944	149	152				
49	G1	930	151	153				
50	B3	944	156	157				
51	C3	944	158	159				
52	H6	032	160					

TYPE	VCC	GRD
930-963	14	7
SN-7401	4	11
SUHL-F23	4	10
F01-F03	4	11
F09	4	11

LBD – SCHEMATIC REF. GATE NO. CONVERSION

LBD	SCH
1-99	1-99
A0-A9	100-109
B0-B9	110-119
C0-C9	120-129
D0-D9	130-139
E0-E9	140-149
F0-F9	150-159
G0-G9	160-169
H0-H9	170-179
I0 -I9	180-189
J0-J9	190-199

LEGEND



D5673

Figure 1-2-2. Columns 1-4 Module Schematic Diagram (Sheet 1 of 2)

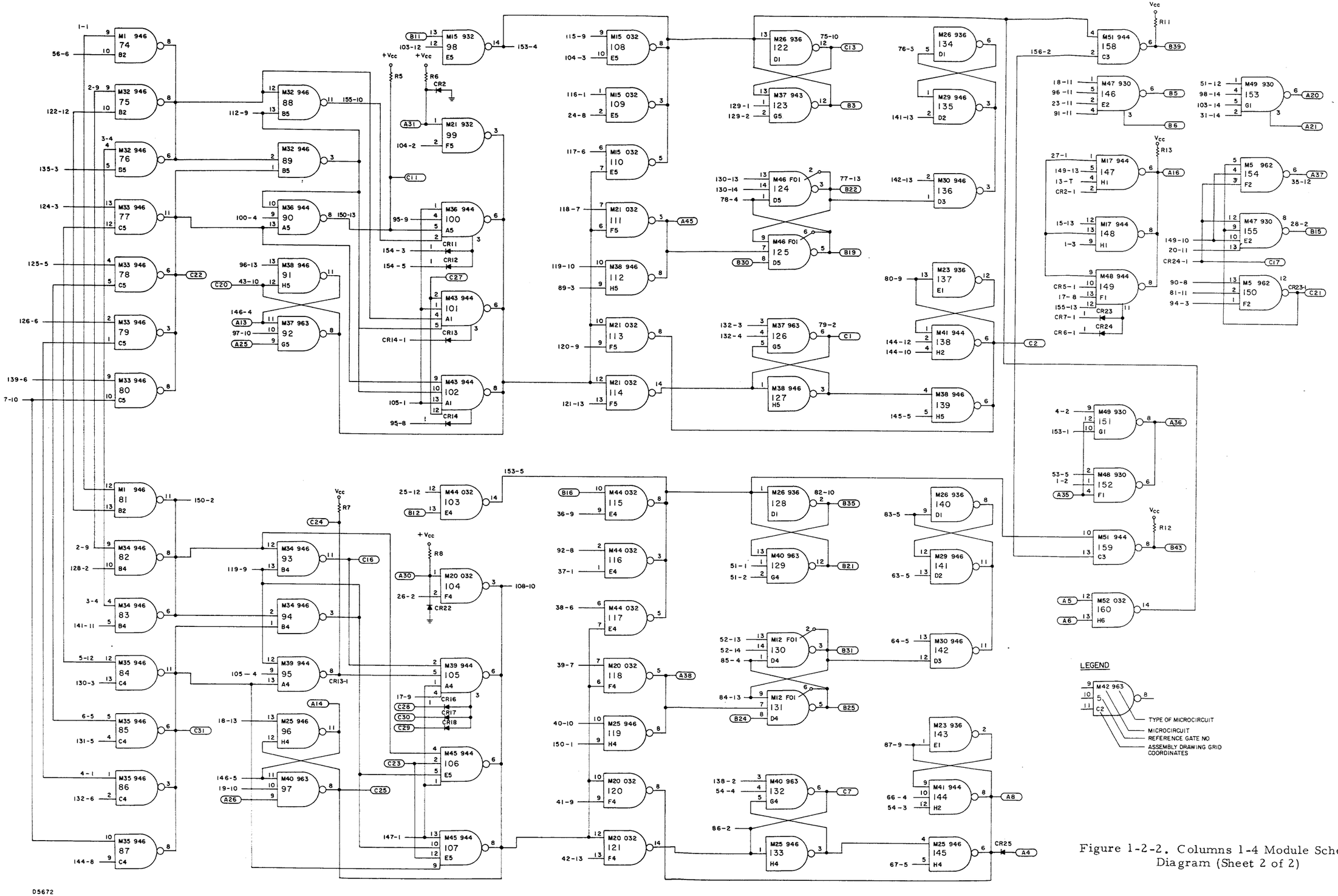


Figure 1-2-2. Columns 1-4 Module Schematic Diagram (Sheet 2 of 2)

05672

COLUMNS A-D MODULE, MODEL CC-365A

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
CR1, CR2, CR13, CR14	DIODE: Replacement type 882	70 943 024 002
CR3-CR12, CR15-CR38	DIODE: Replacement type 1N914	70 943 083 002
M1, M6, M7, M20, M21, M30, M31, M41	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M2, M5, M9, M12, M15, M16, M19, M23, M26, M29, M33, M36, M39, M43, M49	MICROCIRCUIT: 946, quad NAND gate integrated circuit	70 950 105 002
M3, M4, M13, M14, M17, M18, M27, M28, M37, M38, M45, M46	MICROCIRCUIT: 944, power amplifier integrated circuit	70 950 105 008
M8, M22, M42, M32	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70 950 105 012
M35, M48	MICROCIRCUIT: 962, triple NAND gate integrated circuit	70 950 105 006
M10, M25	MICROCIRCUIT: 936, hex inverter integrated circuit	70 950 105 004
M11, M24, M34, M44	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	70 950 100 001
M40, M47, M50	MICROCIRCUIT: 930, dual NAND gate integrated circuit	70 950 105 001
R1, R2, R7 R8	RESISTOR, FIXED, COMPOSITION: 510 ohm ±5%, 1/4W	70 932 007 042
R3-R6	RESISTOR, FIXED, COMPOSITION: 2K ±5%, 1/4W	70 932 007 056

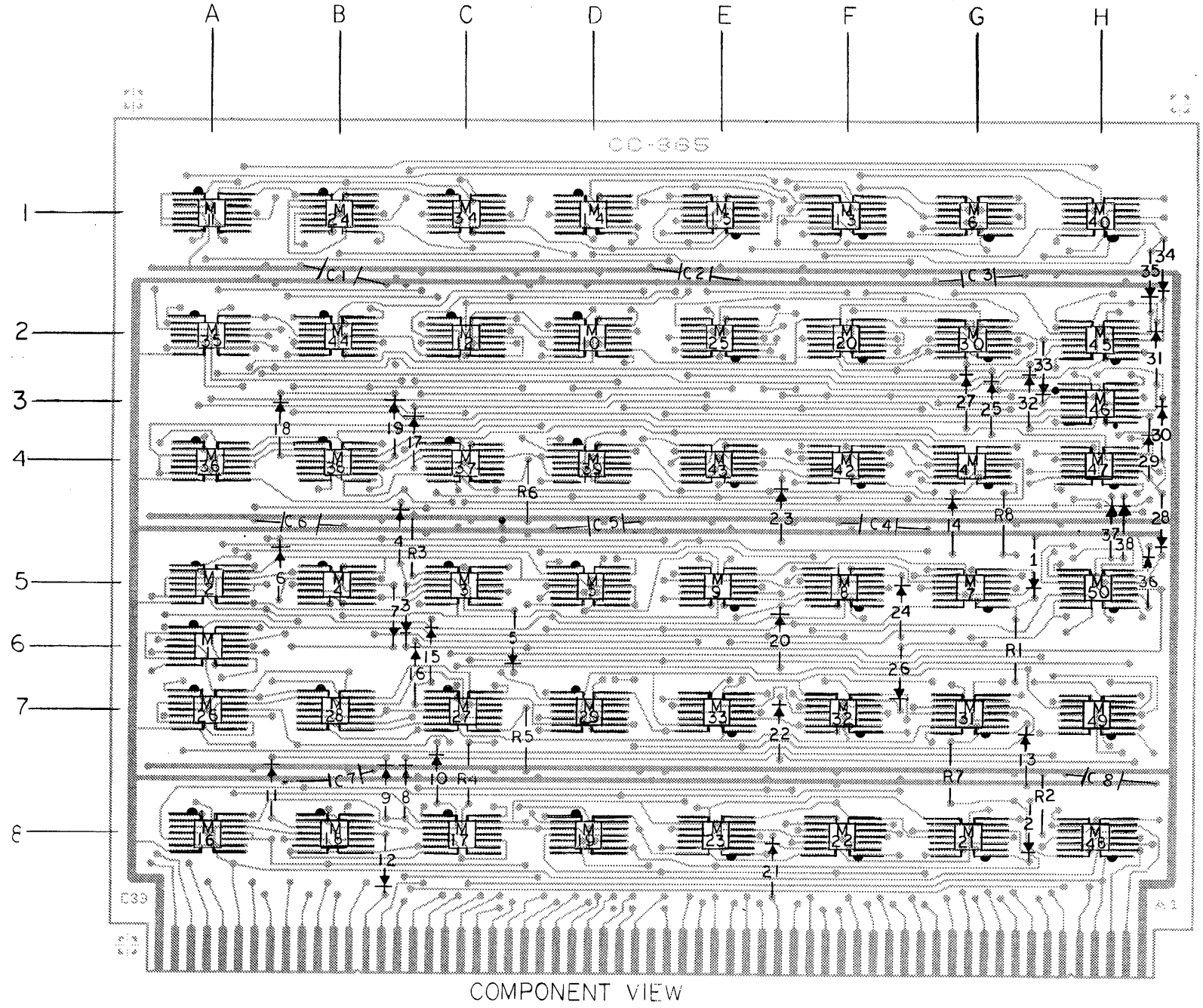


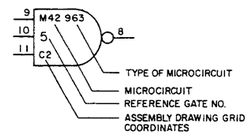
Figure 1-2-3. Columns A-D Module Parts Location

CC 365 Sheet 1

M NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6	7
1	A6	032	1	8	71	78			
2	A5	946	2	3	15	16			
3	C5	944	17	26					
4	B5	944	27	28					
5	D5	946	4	5	6	7			
6	G1	032	33	34	35	40			
7	G5	032	25	36	38	39			
8	F5	963	18	48	51				
9	E5	946	19	37	52	64			
10	D2	936	47	53	59	62	65	68	
11	A1	F01	49	50					
12	C2	946	60	61	66	67			
13	F1	944	133	139					
14	D1	944	63	69					
15	E1	946	130	131	136	137			
16	A8	946	9	10	20	21			
17	C8	944	22	30					
18	B8	944	31	32					
19	D8	946	11	12	13	14			
20	F2	032	41	42	103	104			
21	G8	032	29	43	45	46			
22	F8	963	24	54	57				
23	E8	946	23	44	58	70			
24	B1	F01	55	56					
25	E2	936	117	123	129	132	135	138	
26	A7	946	72	73	85	86			
27	C7	944	87	96					
28	B7	944	97	98					
29	D7	946	74	75	76	77			
30	G2	032	105	110	111	112			
31	G7	963	95	106	108	109			
32	F7	962	89	118	121				
33	E7	946	88	107	122	134			
34	C1	F01	119	120					
35	A2	962	154	157	159				
36	A4	946	79	80	90	91			
37	C4	944	92	100					
38	B4	944	101	102					
39	D4	946	81	82	83	84			
40	H1	930	150	158					
41	G4	032	99	113	115	116			
42	F4	963	94	124	127				
43	E4	946	93	114	128	140			
44	B2	F01	125	126					
45	H2	944	143	156					
46	H3	944	142	144					
47	H4	930	141	146					
48	H8	962	145	147	153				
49	H7	946	148	152	155				
50	H5	930	149	151					

TYPE	VCC	GRD
930-963	14	7
SN-7401	4	11
SUHL-F23	4	10
F01-F03	4	11
F09	4	11

LEGEND



LBD – SCHEMATIC REF. GATE NO. CONVERSION	
LBD	SCH
1-99	1-99
A0-A9	100-109
B0-B9	110-119
C0-C9	120-129
D0-D9	130-139
E0-E9	140-149
F0-F9	150-159
G0-G9	160-169
H0-H9	170-179
I0-I9	180-189
J0-J9	190-199

D5652

Figure 1-2-4. Columns A-D Module Schematic Diagram (Sheet 1 of 2)

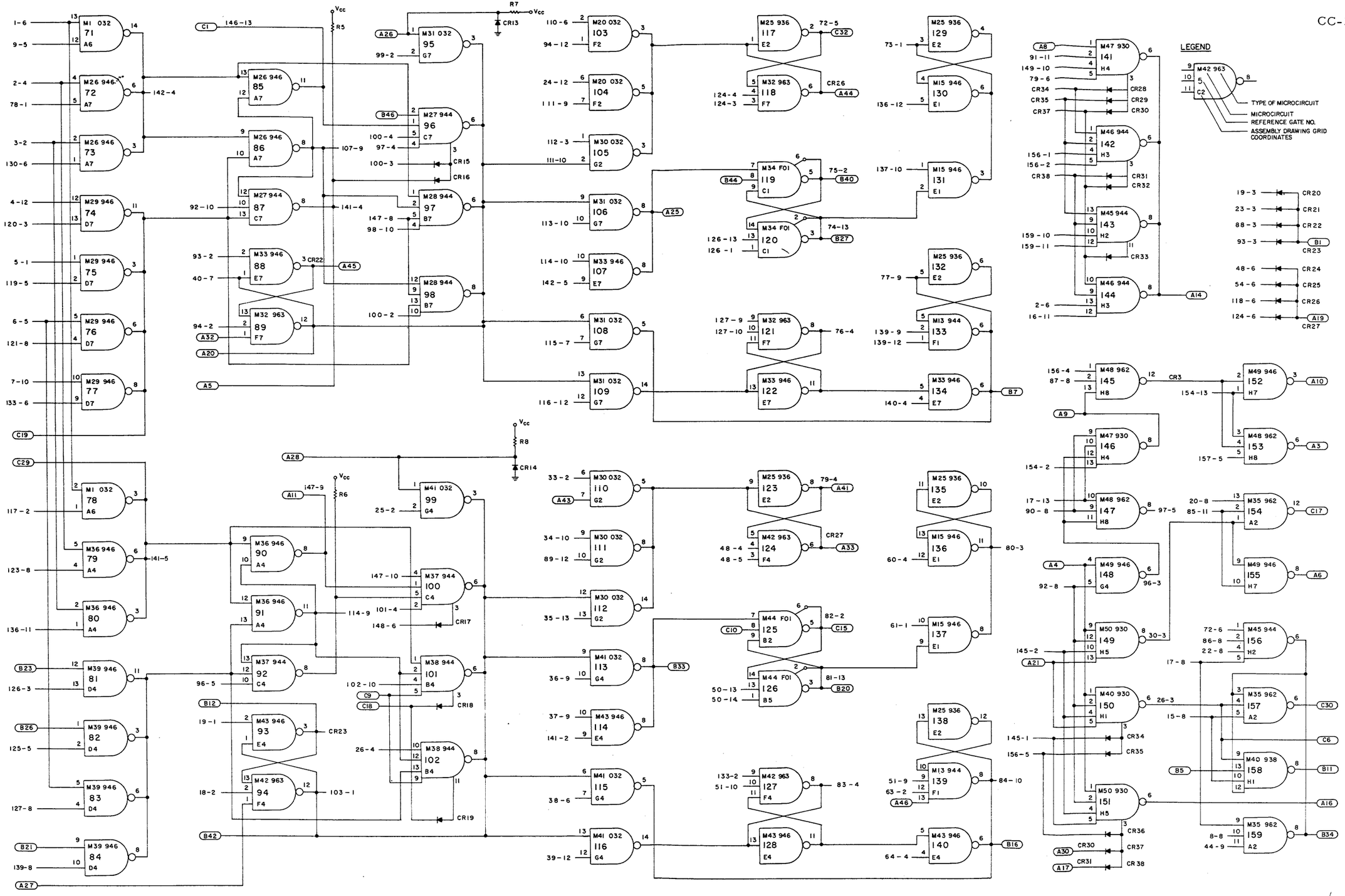


Figure 1-2-4. Columns A-D Module Schematic Diagram (Sheet 2 of 2)

COLUMNS 9-12 MODULE, MODEL CC-366A

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.33 µF ±20%, 50 Vdc	70 930 313 016
CR1, CR4, CR8, CR10	DIODE: Replacement type 882	70 943 024 002
CR2, CR3, CR5-7, CR9, CR11-CR31	DIODE: Replacement type 1N914	70 943 083 002
M1, M2, M5, M9, M12, M15 M16, M19, M23, M26, M29, M33, M36, M39, M43, M49	MICROCIRCUIT: 946, quad NAND gate integrated circuit	70 950 105 002
M6, M7, M30, M41	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M3, M4, M13, M14, M17, M18, M27, M28, M35, M37, M38, M45	MICROCIRCUIT: 944, power amplifier integrated circuit	70 950 105 008
M8, M22, M31, M32, M42	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70 950 105 012
M48	MICROCIRCUIT 962, triple NAND gate integrated circuit	70 950 105 006
M10, M25	MICROCIRCUIT: 936, hex inverter integrated circuit	70 950 105 004
M11, M24, M34, M44	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	70 950 100 001
M46, M47, M40	MICROCIRCUIT: 930, dual NAND gate integrated circuit	70 950 105 001
R1, R3, R5, R7	RESISTOR, FIXED, COMPOSITION: 2K ±5%, 1/4W	70 932 007 056
R2, R4, R6, R8	RESISTOR, FIXED COMPOSITION: 510 ohms ±5%, 1/4W	70 932 007 042

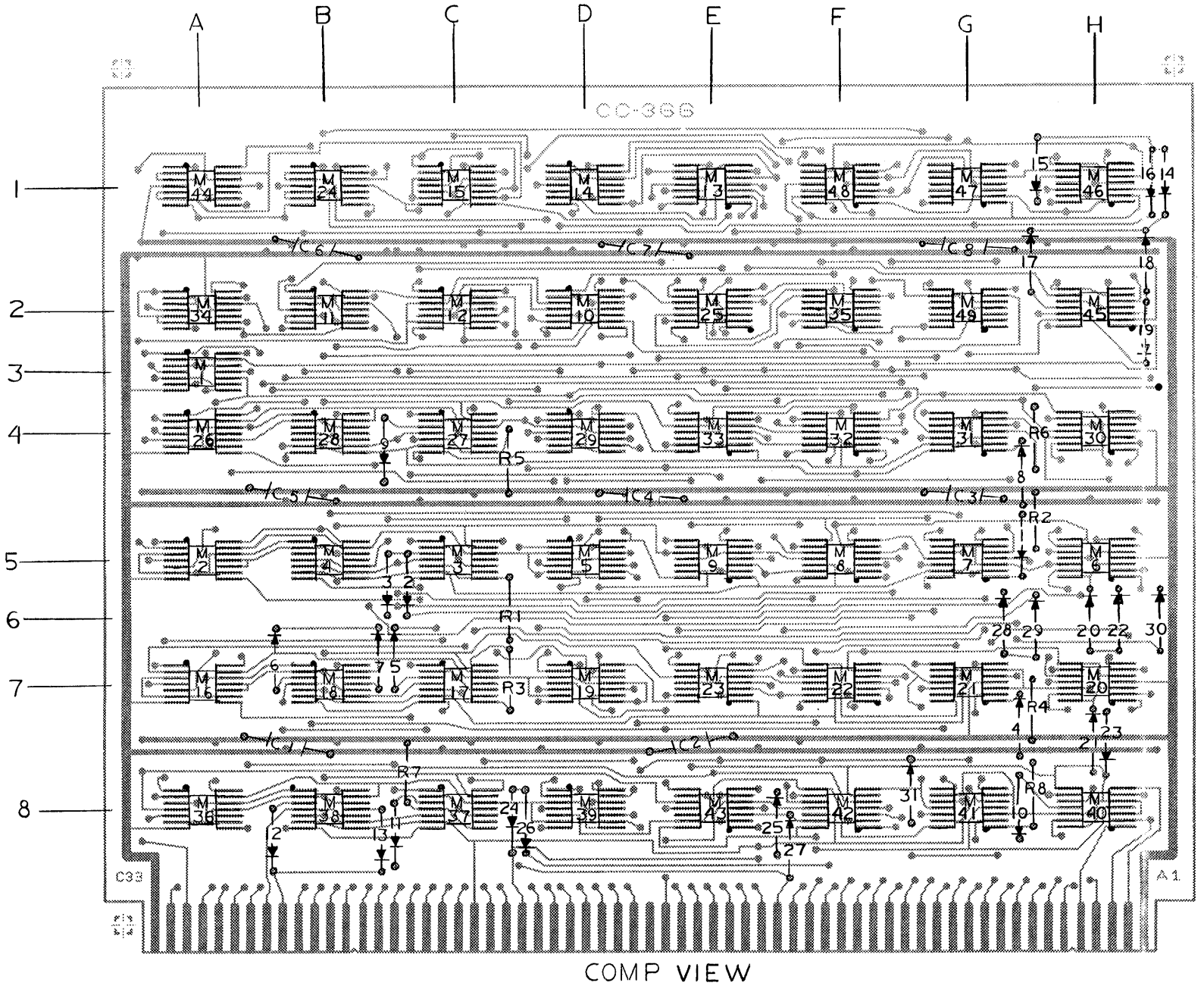
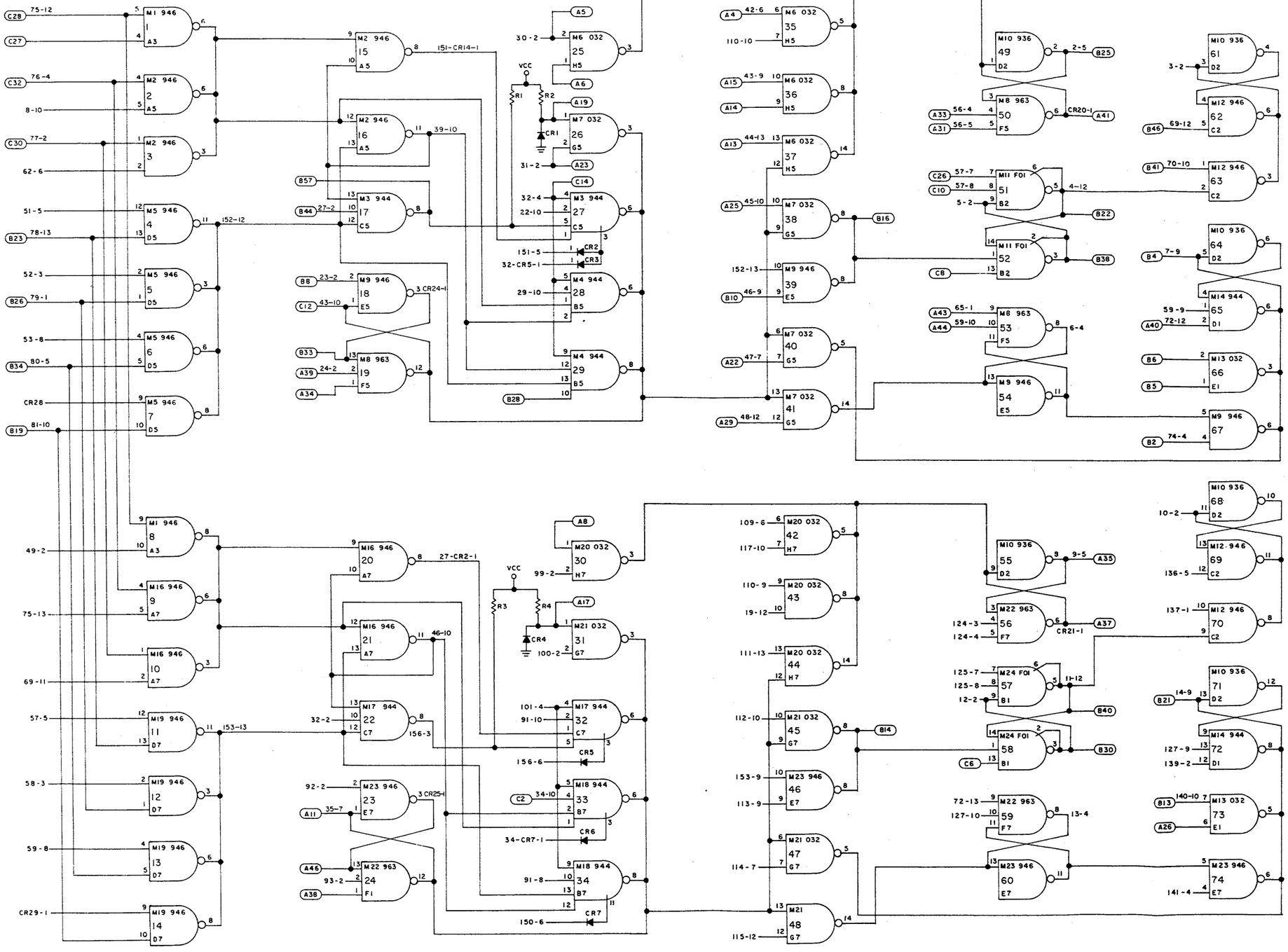


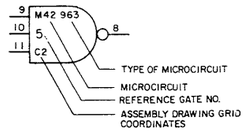
Figure 1-2-5. Columns 9-12 Module Parts Location



M NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6
1	A3	946	1	8	75	82		
2	A5	946	2	3	15	16		
3	C5	944	17	27				
4	B5	944	28	29				
5	D5	946	4	5	6	7		
6	H5	032	25	35	36	37		
7	G5	032	26	38	40	41		
8	F5	963	19	50	53			
9	E5	946	18	39	54	67		
10	D2	936	49	55	61	64	68	71
11	B2	F01	51	52				
12	C2	946	62	63	69	70		
13	E1	032	66	73	140	147		
14	D1	944	65	72				
15	C1	946	136	137	143	144		
16	A7	946	9	10	20	21		
17	C7	944	22	32				
18	B7	944	33	34				
19	D7	946	11	12	13	14		
20	H7	032	30	42	43	44		
21	G7	032	31	45	47	48		
22	F7	963	24	56	59			
23	E7	946	23	46	60	74		
24	B1	F01	57	58				
25	E2	936	123	129	135	138	142	145
26	A4	946	76	77	89	90		
27	C4	944	91	101				
28	B4	944	102	103				
29	D4	946	78	79	80	81		
30	H4	032	99	109	110	111		
31	G4	032	100	112	114	115		
32	F4	963	93	124	127			
33	E4	946	92	113	128	141		
34	A2	F01	125	126				
35	F2	944	139	146				
36	A8	946	83	84	94	95		
37	C8	944	96	106				
38	B8	944	107	108				
39	D8	946	85	86	87	88		
40	H8	032	104	116	117	118		
41	G8	032	105	119	121	122		
42	F8	963	98	130	133			
43	E8	946	97	120	134	148		
44	A1	F01	131	132				
45	H2	944	153	154				
46	H1	930	151	152				
47	G1	930	150					
48	F1	962	149	156	158			
49	G2	946	155	157				

TYPE	VCC	GRD
930-963	14	7
SN-7401	4	11
SUHL-F23	4	10
F01-F03	4	11
F09	4	11

LEGEND



LBD - SCHEMATIC REF. GATE NO. CONVERSION	
LBD	SCH
1-99	1-99
A0-A9	100-109
B0-B9	110-119
C0-C9	120-129
D0-D9	130-139
E0-E9	140-149
F0-F9	150-159
G0-G9	160-169
H0-H9	170-179
I0-I9	180-189
J0-J9	190-199

Figure 1-2-6. Columns 9-12 Module Schematic Diagram (Sheet 1 of 2)

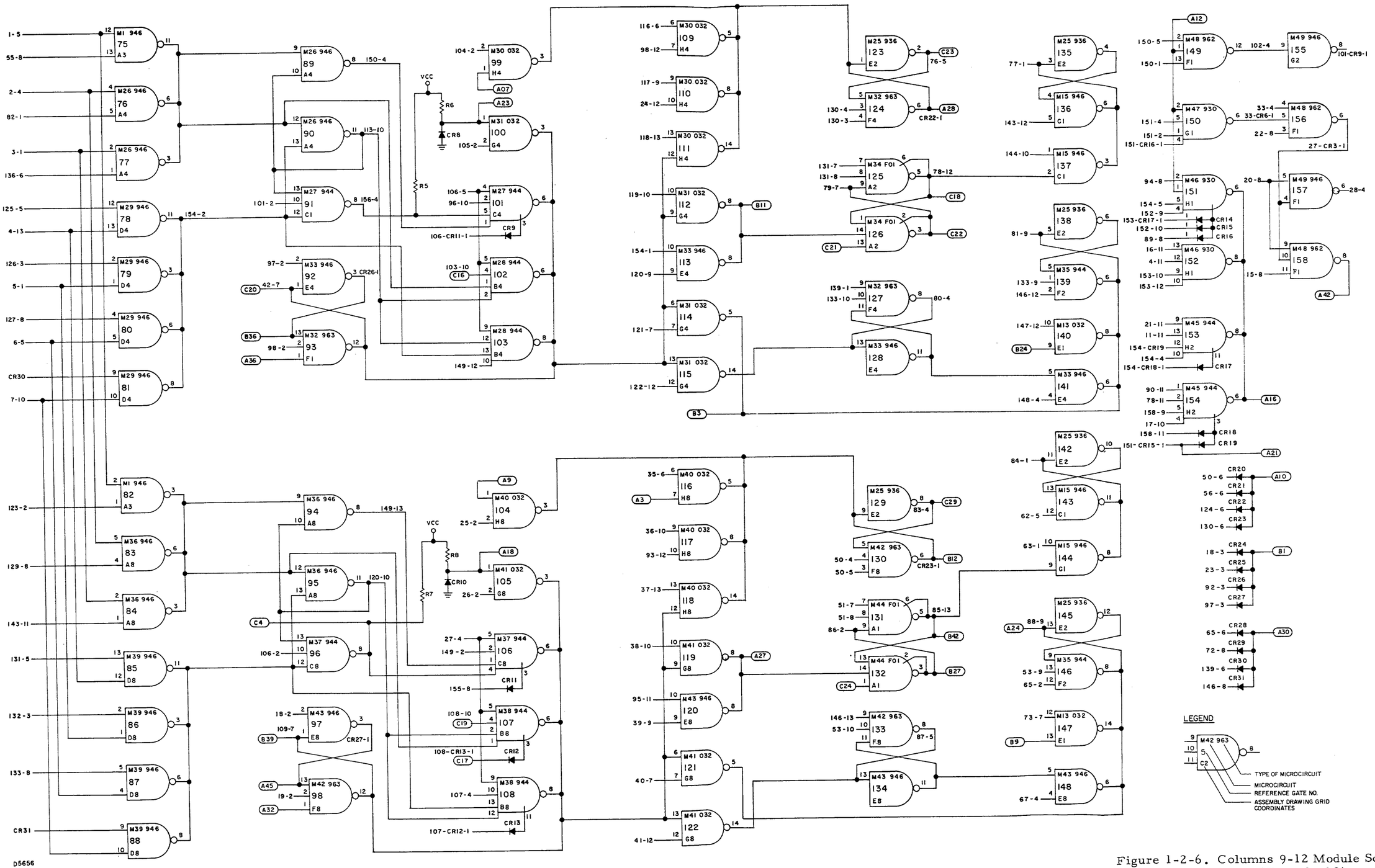
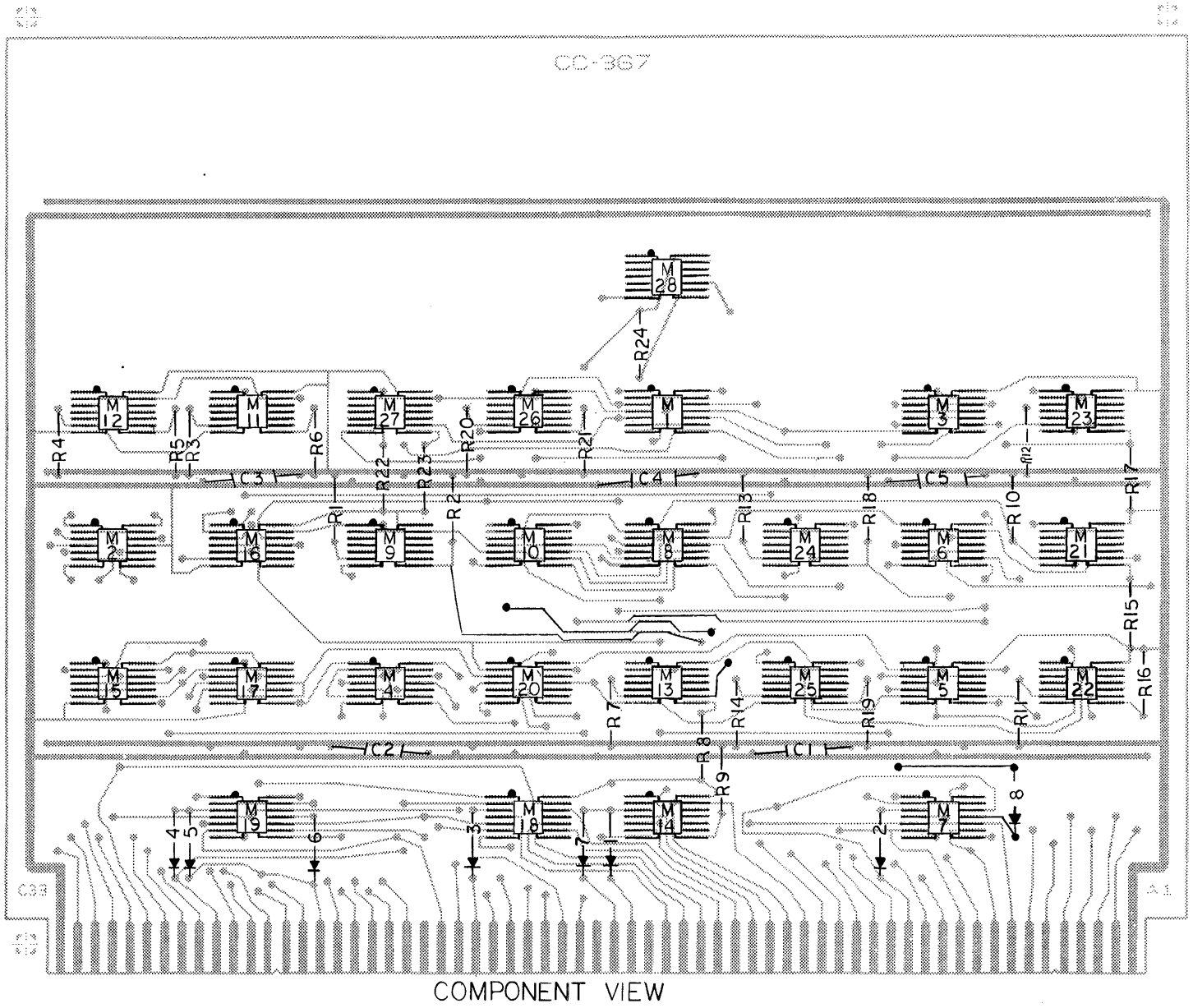


Figure 1-2-6. Columns 9-12 Module Schematic Diagram (Sheet 2 of 2)

ADDRESS BUS MODULE, MODEL CC-367

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C5	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
CR1-CR8	DIODE: Replacement type 1N914	70 943 083 002
M1, M2, M4, M20	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M3, M16, M17	MICROCIRCUIT: 949, quad NAND gate integrated circuit	70 950 105 010
M5, M8	MICROCIRCUIT: 937, fast hex inverter integrated circuit	70 950 105 011
M6, M7, M18, M19	MICROCIRCUIT: 961, dual NAND gate integrated circuit	70 950 105 009
M9, M11-M14, M21-M28	MICROCIRCUIT: 944, power amplifier integrated circuit	70 950 105 008
M10, M15	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70 950 105 012
R1-R9	RESISTOR, FIXED, COMPOSITION: 2K ±5%, 1/4W	70 932 007 056
R10-R24	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4W	70 932 007 049



COMPONENT VIEW

Figure 1-2-7. Address Bus Module Parts Location

CC-367 Sheet 1

M NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6
1	E4	032	1	2	3	4		
2	A5	032	8	9	10	11		
3	G4	949	16	17	18	20		
4	C7	032	22	23	29	30		
5	G7	937	12	13	15	17	69	
6	G5	961	5	26				
7	G8	961	7	24				
8	E5	937	25	27	34	36	37	42
9	C5	944	31	32				
10	D5	963	33	41				
11	B4	944	35	40				
12	A4	944	38	39				
13	E7	944	43	44				
14	E8	944	45	70				
15	A7	963	21	51	52			
16	B5	949	6	50	62			
17	B7	949	46	47	48	53		
18	D8	961	28	54				
19	B8	961	55	56				
20	D7	032	14	49	63			
21	H5	944	57	64				
22	H7	944	58	65				
23	H4	944	59	63				
24	F5	944	60	67				
25	F7	944	61	68				
26	D4	944	71	72				
27	C4	944	73	74				
28	E2	944	75					

LBD – SCHEMATIC REF. GATE NO. CONVERSION	
LBD	SCH
1-99	1-99
A0-A9	100-109
B0-B9	110-119
C0-C9	120-129
D0-D9	130-139
E0-E9	140-149
F0-F9	150-159
G0-G9	160-169
H0-H9	170-179
I0-I9	180-189
J0-J9	190-199

TYPE	V_{cc}	GND
930-963	14	7
SN-7401	4	11
F-01-F-09	4	11
F-23	4	11

LEGEND

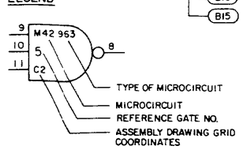


Figure 1-2-8. Address Bus Module Schematic Diagram

SHIFT REGISTER MODULE, MODEL CC-368

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
CR1, CR3-CR14	DIODE: Replacement type 1N914	70 943 083 002
M1, M5, M7, M8, M11, M14, M15, M18, M20, M22, M25, M28, M29, M33, M35, M37, M41, M42	MICROCIRCUIT: 946, quad NAND gate integrated circuit	70 950 105 002
M2, M9, M16, M23, M31, M38	MICROCIRCUIT: 936, hex inverter integrated circuit	70 950 105 004
M3, M6, M10, M13, M17, M19, M24, M26, M32, M34, M39, M40	MICROCIRCUIT: 962, triple NAND gate integrated circuit	70 950 105 006
M4, M12, M21, M27, M30, M36	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M43	MICROCIRCUIT: 932, power amplifier integrated circuit	70 950 105 005
M44	MICROCIRCUIT: 930, dual NAND gate integrated circuit	70 950 105 001
M45-M50	MICROCIRCUIT: F-04, flip-flop integrated circuit	70 950 100 004
M51-M54	MICROCIRCUIT: 944, power amplifier integrated circuit	70 950 105 008
R1, R2	RESISTOR,FIXED, COMPOSITION: 2K ±5%, 1/4W	70 932 007 056
R3-R10	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4W	70 932 007 049

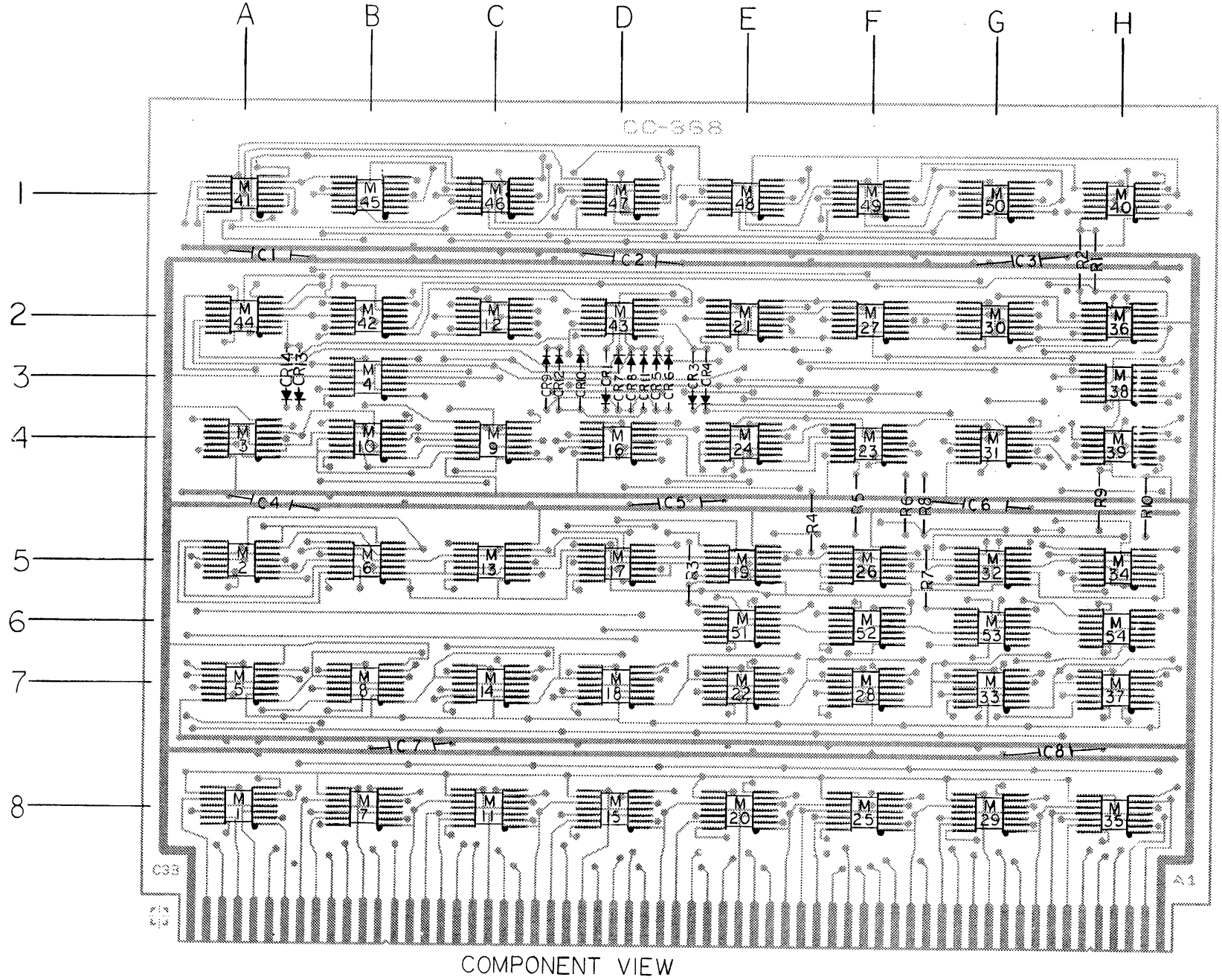
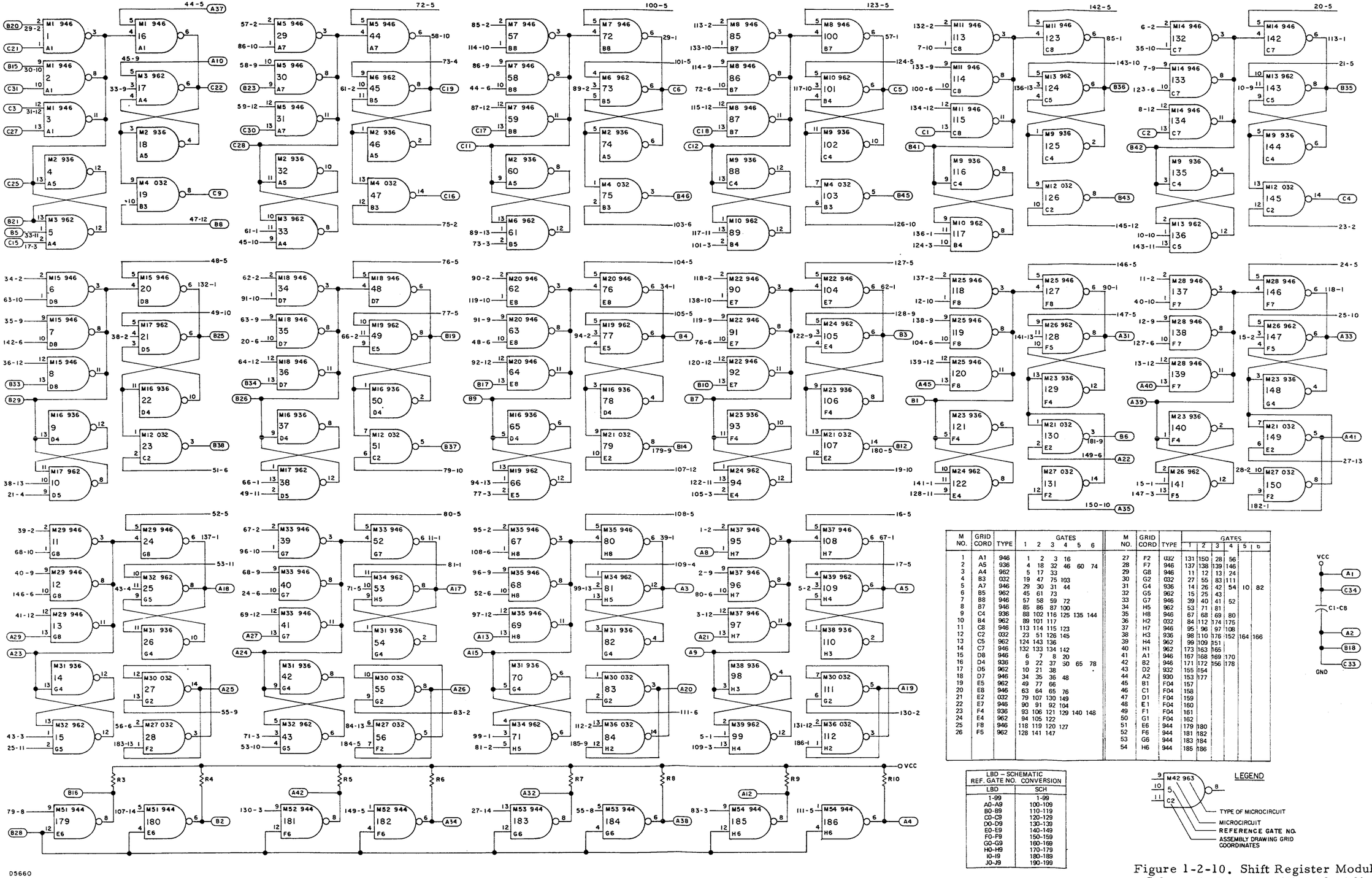


Figure 1-2-9. Shift Register Module Parts Location



D5660

M NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6
1	A1	946	1	2	3	16		
2	A5	936	4	18	32	46	60	74
3	A4	962	5	17	33			
4	B3	032	19	47	75	103		
5	A7	946	29	30	31	44		
6	B5	962	45	61	73			
7	B8	946	57	58	59	72		
8	B7	946	85	86	87	100		
9	C4	936	88	102	116	125	135	144
10	B4	962	89	101	117			
11	C8	946	113	114	115	123		
12	C2	032	23	51	126	145		
13	C5	962	124	143	136			
14	C7	946	132	133	134	142		
15	D8	946	6	7	8	20		
16	D4	936	9	22	37	30	65	78
17	D5	962	10	21	38			
18	D7	946	34	35	36	48		
19	E5	962	49	77	66			
20	E8	946	63	64	65	76		
21	E2	032	79	107	130	149		
22	E7	946	90	91	92	104		
23	F4	936	93	106	121	129	140	148
24	E4	962	94	105	122			
25	F8	946	118	119	120	127		
26	F5	962	128	141	147			

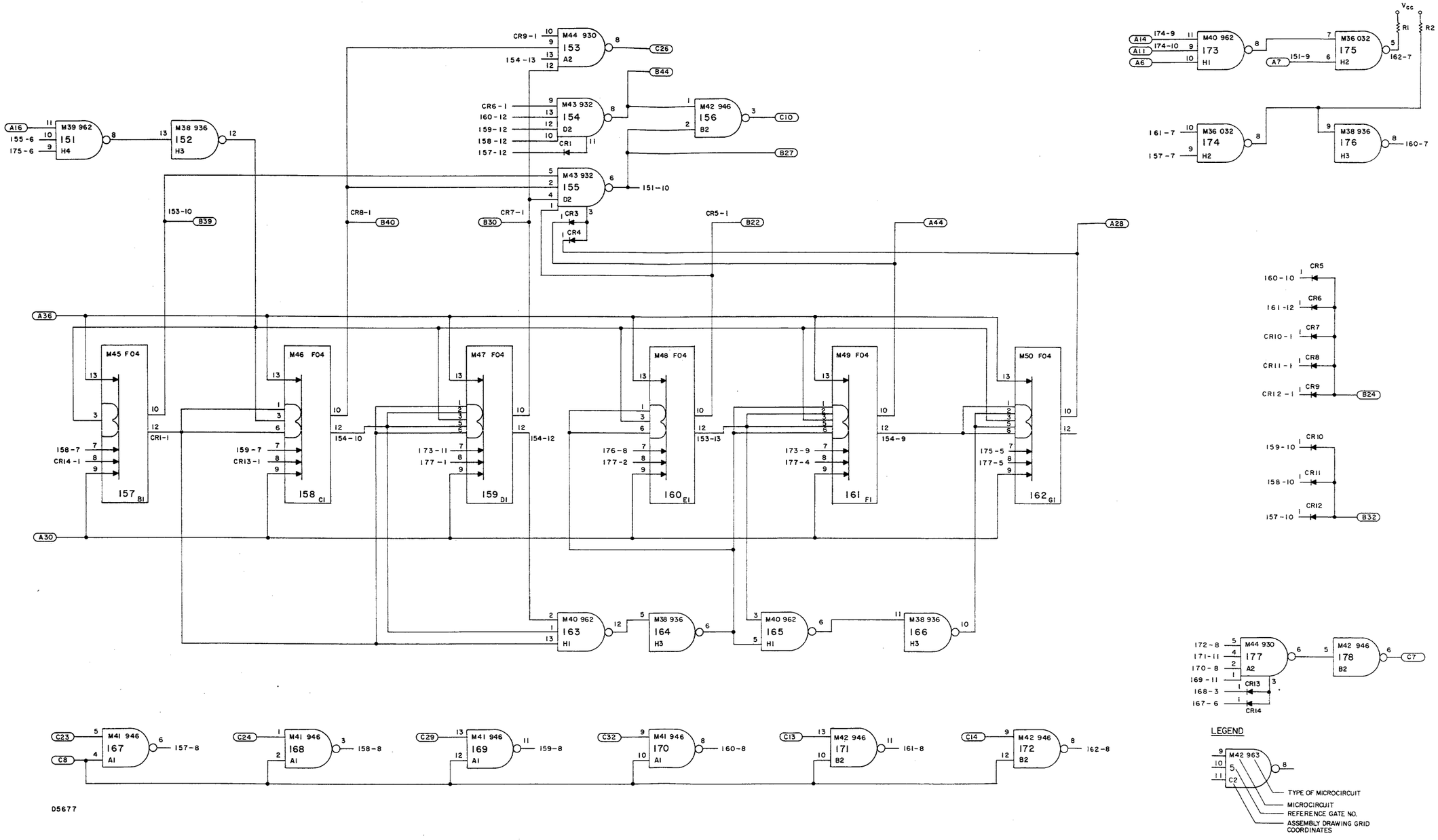
M NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6
27	F2	032	131	150	28	56		
28	F7	946	137	138	139	146		
29	G8	946	11	12	13	24		
30	G2	032	27	55	83	111		
31	G4	936	14	26	42	54	10	82
32	G5	962	15	25	43			
33	G7	946	39	40	41	52		
34	H5	962	53	71	81			
35	H8	946	67	68	69	80		
36	H2	032	84	112	174	175		
37	H7	946	95	96	97	108		
38	H3	936	98	110	176	152	164	166
39	H4	962	99	109	151			
40	H1	962	173	163	165			
41	A1	946	167	168	169	170		
42	B2	946	171	172	156	178		
43	D2	932	155	154				
44	A2	930	153	177				
45	B1	F04	157					
46	C1	F04	158					
47	D1	F04	159					
48	E1	F04	160					
49	F1	F04	161					
50	G1	F04	162					
51	E6	944	179	180				
52	F6	944	181	182				
53	G6	944	183	184				
54	H6	944	185	186				

LBD	SCH
1-99	1-99
A0-A9	100-109
B0-B9	110-119
C0-C9	120-129
D0-D9	130-139
E0-E9	140-149
F0-F9	150-159
G0-G9	160-169
H0-H9	170-179
I0-I9	180-189
J0-J9	190-199

LBD – SCHEMATIC REF. GATE NO. CONVERSION

LEGEND

Figure 1-2-10. Shift Register Module Schematic Diagram (Sheet 1 of 2)



LEGEND

Figure 1-2-10. Shift Register Module Schematic Diagram (Sheet 2 of 2)

LAMP DRIVER MODULE, MODEL CC-369B

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
CR1-CR19, CR20A-CR20S, CR21-CR23	DIODE: Replacement type 1N914	70 943 083 002
M1-M16	MICROCIRCUIT: 936, hex inverter integrated circuit	70 950 105 004
M18-M20	MICROCIRCUIT: 937, fast hex inverter integrated circuit	70 950 105 011
M21, M22, M25	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M23, M17	MICROCIRCUIT: 949, quad NAND gate integrated circuit	70 950 105 010
M24	MICROCIRCUIT: 961, dual NAND gate integrated circuit	70 950 105 009
Q1A-Q1S, Q2	TRANSISTOR, SILICON, NPN:	70 943 744 003
R1A-R1P	RESISTOR, FIXED, COMPOSITION: 2K ±5%, 1/4W	70 932 007 056
R2A-R2S, R7,	RESISTOR, FIXED, FILM: 1.1K ±1%, 1/2W	70 932 123 203
R3A-R3S, R4	RESISTOR, FIXED, COMPOSITION: 820 ohms ±5%, 1/4W	70 932 007 047
R5, R9-R12	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4W	70 932 007 049
R6	RESISTOR, FIXED, FILM: 100 ohms ±1%, 1/2W	70 932 123 101

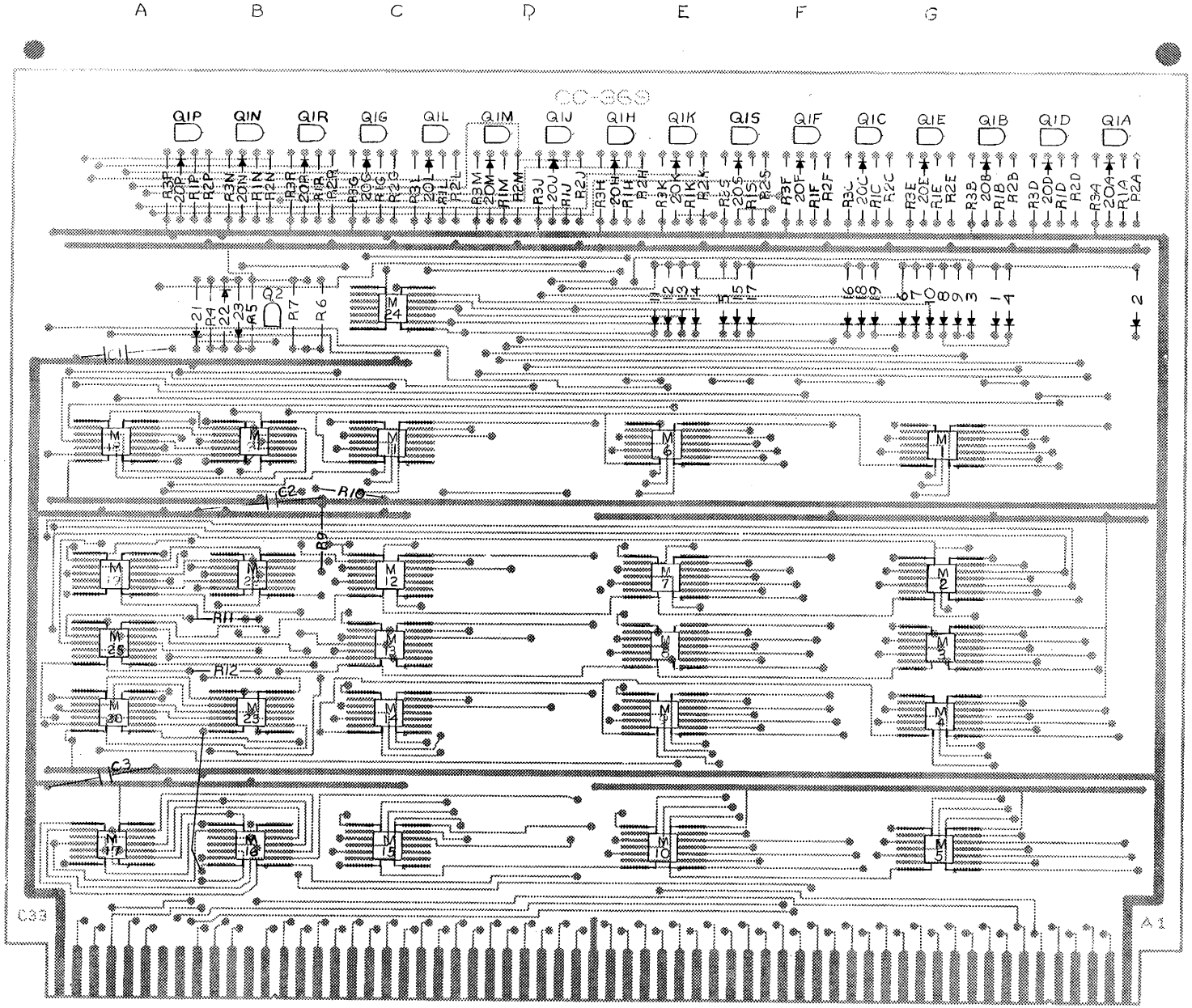


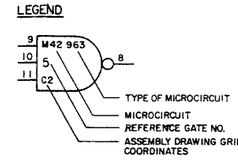
Figure 1-2-11. Lamp Driver Module Parts Location

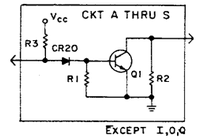
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	TAKEN FROM S.R. 54-3320	—	—
B	CHGS/ECO 9313	DMH 9/21/71	J WAGNER 9/21/71
C	ECO 9919 SSR	11/23/71	
D	CHG'D PER ECO 20593	7-8 9/21/72	

LBD — SCHEMATIC REF. GATE NO. CONVERSION

LBD	SCH
1-99	1-99
A0-A9	100-109
B0-B9	110-119
C0-C9	120-129
D0-D9	130-139
E0-E9	140-149
F0-F9	150-159
G0-G9	160-169
H0-H9	170-179
I0-I9	180-189
J0-J9	190-199

LEGEND





M NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6
1	G4	936	1	6	11	16	21	26
2	G5	936	2	7	12	17	22	27
3	G6	936	3	8	13	18	23	28
4	G7	936	4	9	14	19	24	29
5	G8	936	5	10	15	20	25	30
6	E4	936	31	36	41	46	51	56
7	E5	936	32	37	42	47	52	57
8	E6	936	33	38	43	48	53	58
9	E7	936	34	39	44	49	54	59
10	E8	936	35	40	45	50	55	60
11	C4	936	61	66	71	76		
12	C5	936	62	67	72	77		
13	C6	936	63	68	73	78		
14	C7	936	64	69	74	79		
15	C8	936	65	70	75	80		
16	B8	936	85	86	87	88	91	
17	A8	949	93	94	123	124		
18	A4	937	95	96	97	98	99	102
19	A5	937	100	101	103	104	105	
20	A7	937	82	83	84	106	107	117
21	B4	032	108	109	110	111		
22	B5	032	112	113	114	115		
23	B7	949	89	90	116			
24	C2	961	81					
25	A6	032	119	120	121	122		
26								
27								
28								
29								
30								

05653

Figure 1-2-12. Lamp Driver Module Schematic Diagram (Sheet 1 of 2)

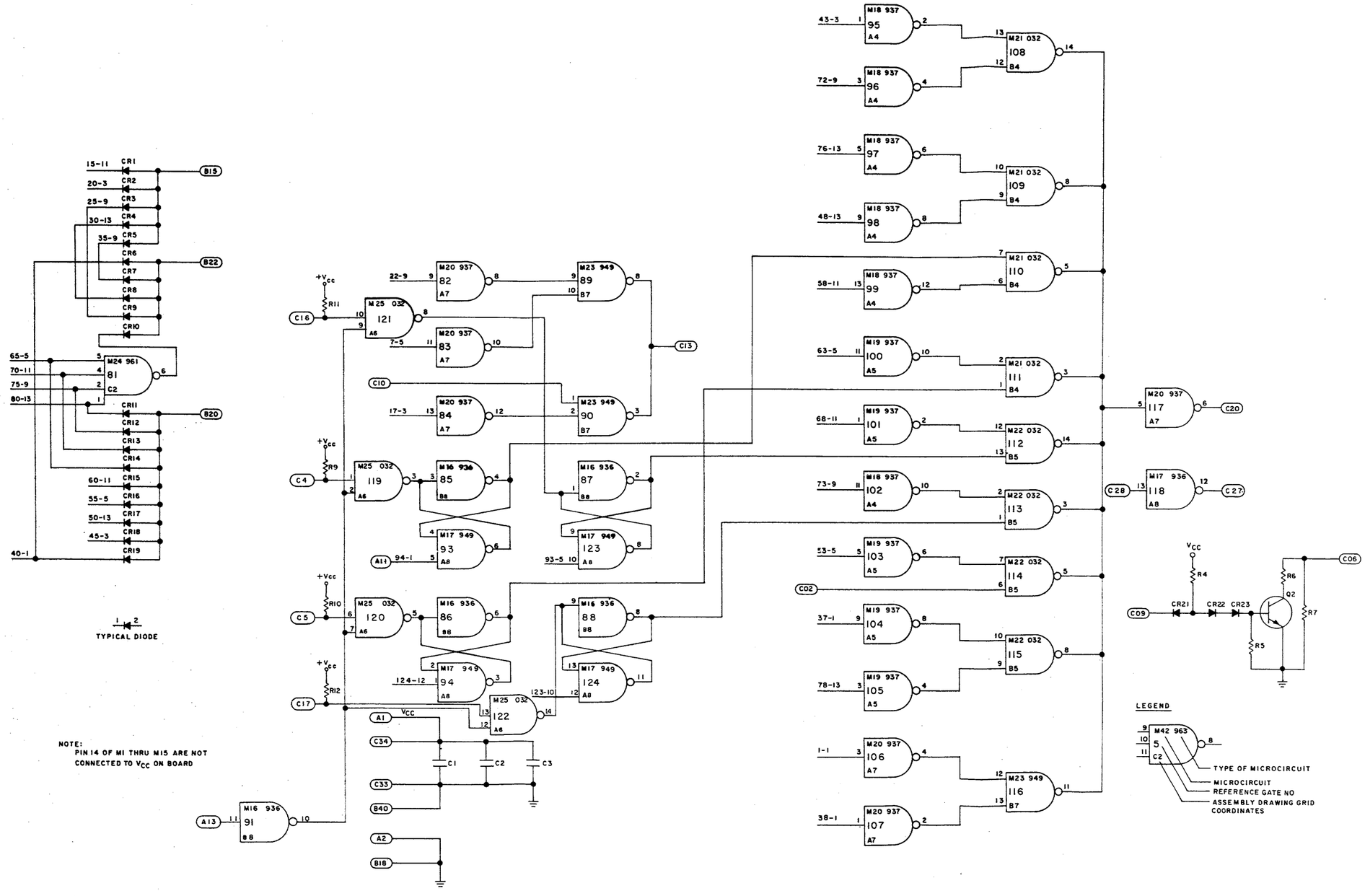


Figure 1-2-12. Lamp Driver Module Schematic Diagram (Sheet 2 of 2)

M REGISTER MODULE, MODEL CC-370

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
CR1-CR27	DIODE: Replacement type 1N914	70 943 083 002
M1, M7, M10, M22, M33, M48	MICROCIRCUIT: 937, fast hex inverter integrated circuit	70 950 105 011
M2, M18	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M3, M6, M9	MICROCIRCUIT: F-09, dual power amplifier integrated circuit	70 950 100 009
M4, M14, M15, M25, M31, M38, M42	MICROCIRCUIT: 949, quad NAND gate integrated circuit	70 950 105 010
M5, M8, M11, M12, M24, M26, M32, M36, M41, M46, M49	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70 950 105 012
M13, M20, M21, M29, M30, M35, M39, M40, M43, M44, M45	MICROCIRCUIT: 961, dual NAND gate integrated circuit	70 950 105 009
M16, M17, M19, M23, M27, M28, M34, M37, M47	MICROCIRCUIT: 944, power amplifier integrated circuit	70 950 105 008
R1-R11	RESISTOR, FIXED, COMPOSITION: 2K ±5%, 1/4W	70 932 007 056

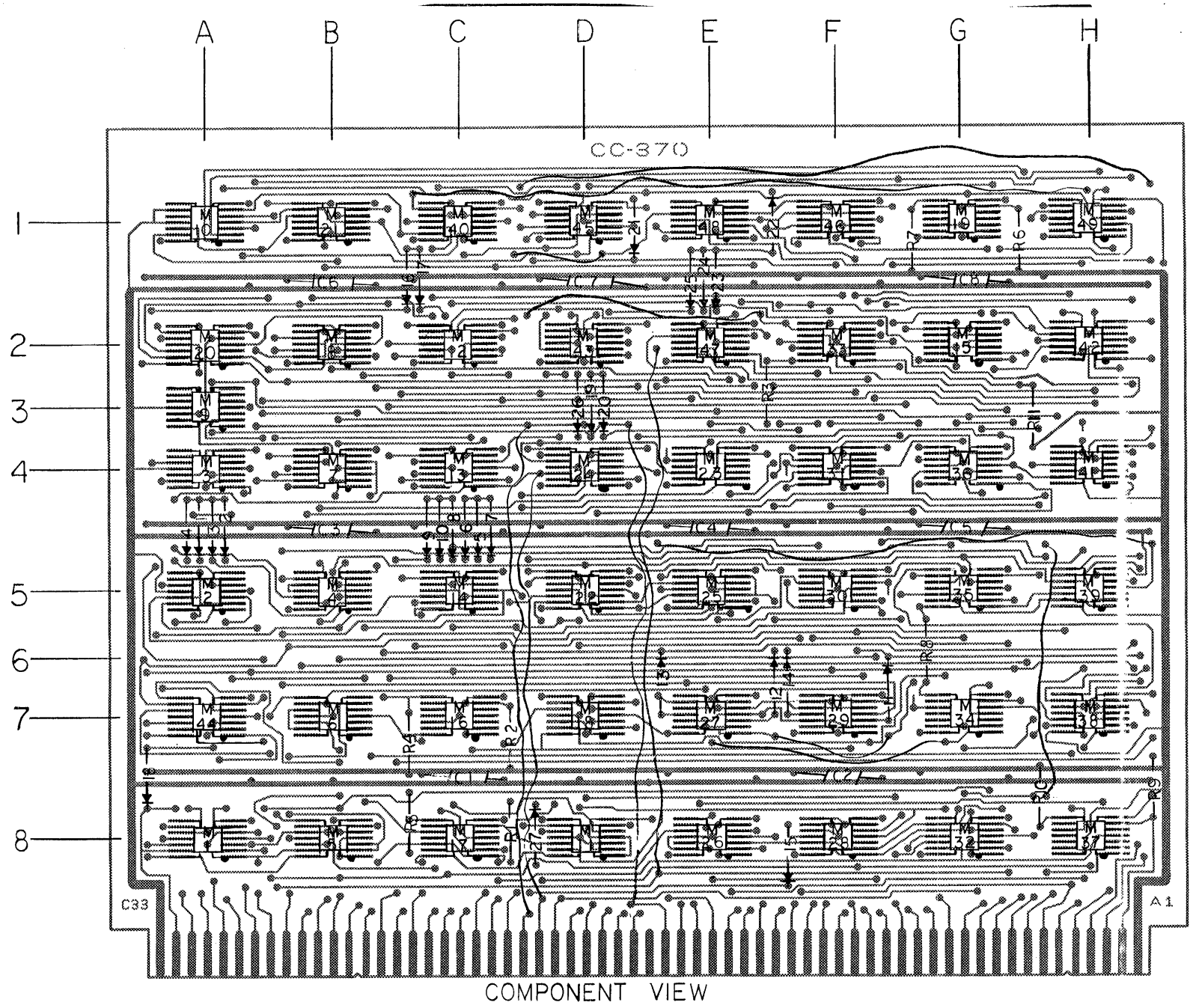
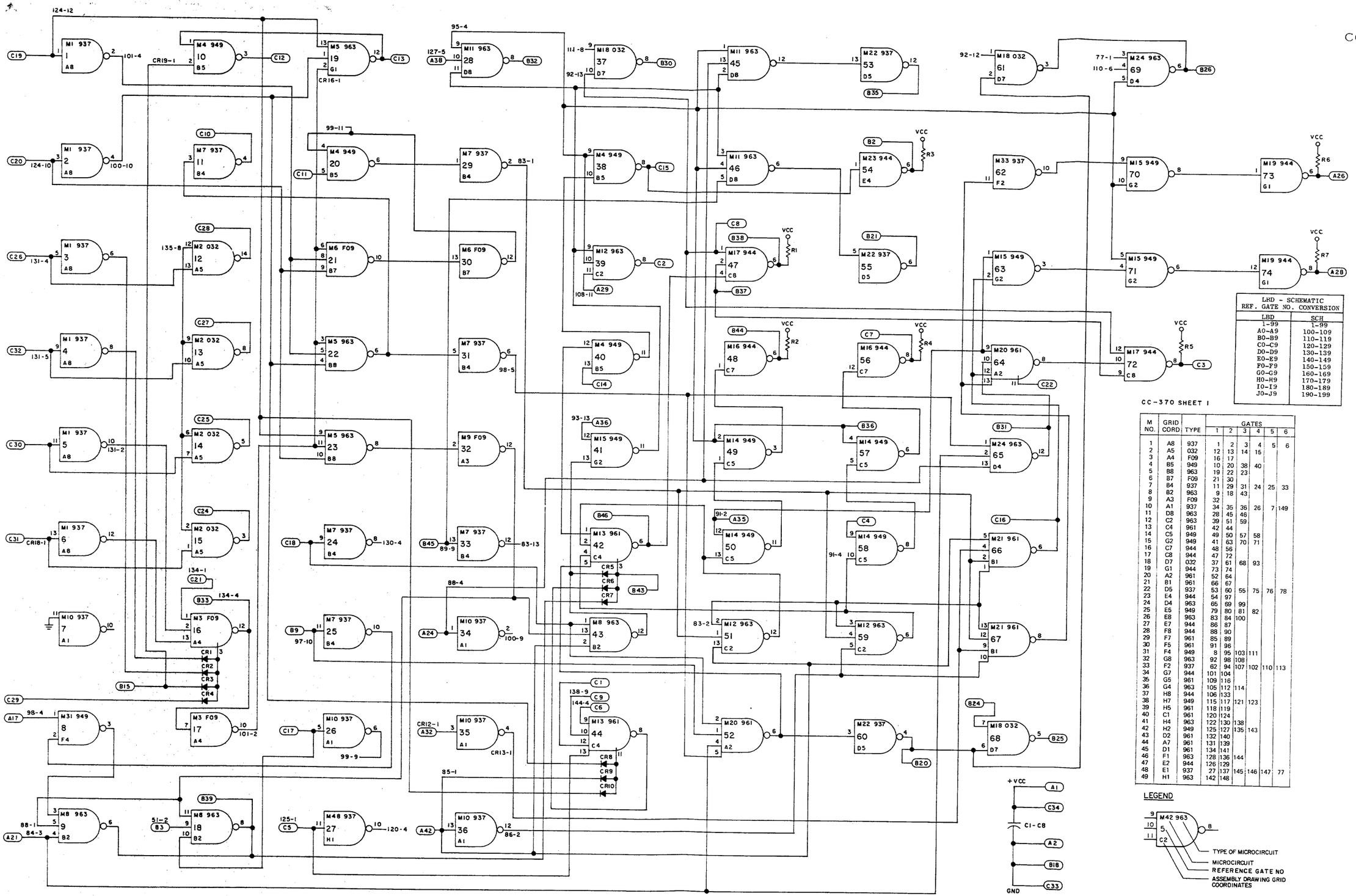


Figure 1-2-13. M Register Module Parts Location



LBD - SCHEMATIC REF. GATE NO. CONVERSION

LBD	SCH
1-99	1-99
A0-A9	100-109
B0-B9	110-119
C0-C9	120-129
D0-D9	130-139
E0-E9	140-149
F0-F9	150-159
G0-G9	160-169
H0-H9	170-179
I0-I9	180-189
J0-J9	190-199

CC-370 SHEET 1

M NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6
1	A8	937	1	2	3	4	5	6
2	A5	032	12	13	14	15		
3	A4	F09	16	17				
4	B5	949	10	20	38	40		
5	B8	963	19	22	23			
6	B7	F09	21	30				
7	B4	937	11	29	31	24	25	33
8	B2	963	9	18	43			
9	A3	F09	32					
10	A1	937	34	35	36	26	7	149
11	D8	963	28	45	46			
12	C2	963	39	51	59			
13	C4	961	42	44				
14	C5	949	49	50	57	58		
15	G2	949	41	63	70	71		
16	C7	944	48	56				
17	C8	944	47	72				
18	D7	032	37	61	68	93		
19	G1	944	73	74				
20	A2	961	52	64				
21	B1	961	66	67				
22	D5	937	53	60	55	75	76	78
23	E4	944	54	97				
24	D4	963	65	69	99			
25	E5	949	79	80	81	82		
26	E8	963	83	84	100			
27	E7	944	86	87				
28	F8	944	88	90				
29	F7	961	85	89				
30	F5	961	91	96				
31	F4	949	8	95	103	111		
32	G8	963	92	98	108			
33	F2	937	62	94	107	102	110	113
34	G7	944	101	104				
35	G5	961	109	116				
36	G4	963	105	112	114			
37	H8	944	106	133				
38	H7	949	115	117	121	123		
39	H5	961	118	119				
40	C1	961	120	124				
41	H4	963	122	130	138			
42	H2	949	125	127	135	143		
43	D2	961	132	140				
44	A7	961	131	139				
45	D1	961	134	141				
46	F1	963	128	136	144			
47	E2	944	126	129				
48	E1	937	27	137	145	146	147	77
49	H1	963	142	148				

Figure 1-2-14. M Register Module Schematic Diagram (Sheet 1 of 2)

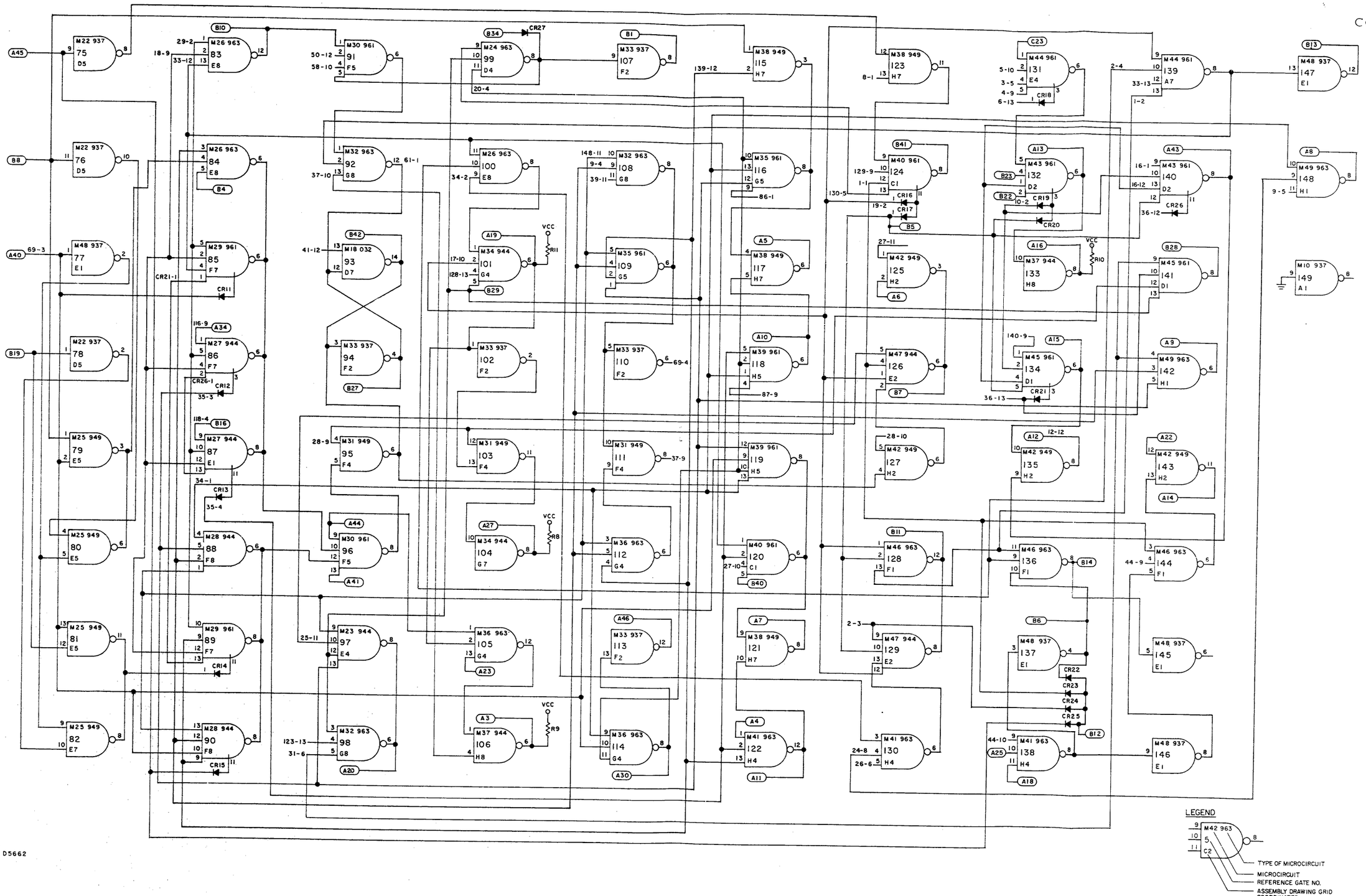


Figure 1-2-14. M Register Module Schematic Diagram (Sheet 2 of 2)

CLOCK MODULE, MODEL CC-371

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C24	CAPACITOR, FIXED, MICA DIELECTRIC: 75 pF ±2%, 100 Vdc	70 930 004 214
C25-C32	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
CR1-CR29	DIODE: Replacement type 1N914	70 943 083 002
L1-L3	DELAY LINE	70 000 206 703
M1-M8, M13-M15, M18, M19, M26	MICROCIRCUIT: 961, dual NAND gate integrated circuit	70 950 105 009
M9, M17, M21, M22, M24, M30, M35	MICROCIRCUIT: 944, power amplifier integrated circuit	70 950 105 008
M10, M20, M23, M27 M29, M31	MICROCIRCUIT: 949, quad NAND gate integrated circuit	70 950 105 010
M11, M25, M28, M42	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70 950 105 012
M12, M33	MICROCIRCUIT: 937, hex inverter integrated circuit	70 950 105 011
M16	MICROCIRCUIT: F-19, logic gate integrated circuit	70 950 100 019
M32, M34	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M36-M41, M43-M50	MICROCIRCUIT: F-09, power amplifier integrated circuit	70 950 100 009
R1	RESISTOR, FIXED, COMPOSITION: 130 ohms ±5%, 1/4W	70 932 007 028
R2-R9	RESISTOR, FIXED, COMPOSITION: 2K ±5%, 1/4W	70 932 007 056
R10	RESISTOR, FIXED, COMPOSITION: 510 ohms ±5%, 1/4W	70 932 007 042

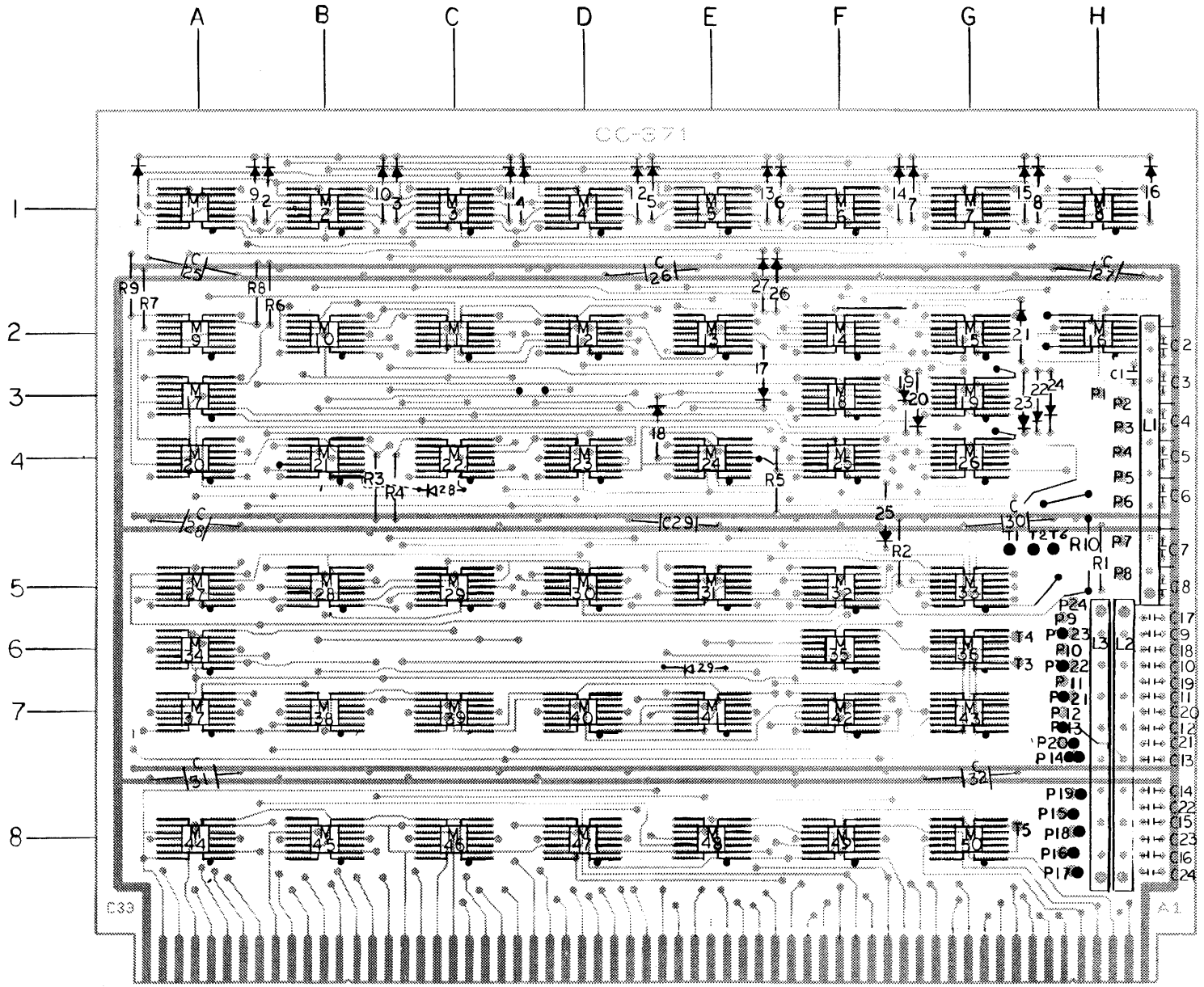
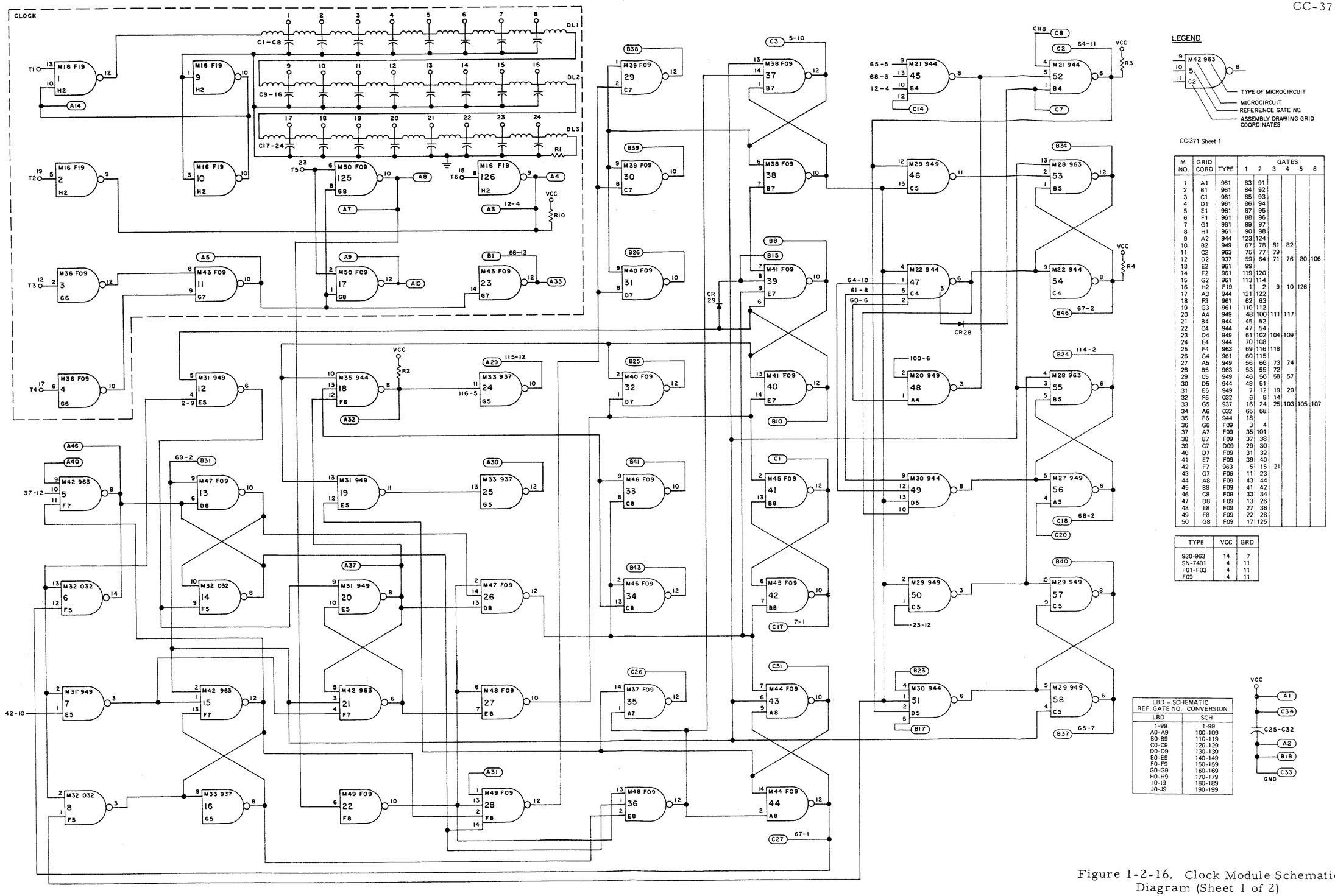


Figure 1-2-15. Clock Module Parts Location



CC-371 Sheet 1

M. NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6
1	A1	961	83	91				
2	B1	961	84	92				
3	C1	961	85	93				
4	D1	961	86	94				
5	E1	961	87	95				
6	F1	961	88	96				
7	G1	961	89	97				
8	H1	961	90	98				
9	A2	944	123	124				
10	B2	949	67	78	81	82		
11	C2	963	75	77	79			
12	D2	937	59	64	71	76	80	106
13	E2	961	99					
14	F2	961	119	120				
15	G2	961	113	114				
16	H2	F19	1	2	9	10	126	
17	A3	944	121	122				
18	F3	961	62	63				
19	G3	961	110	112				
20	A4	949	48	100	111	117		
21	B4	944	45	52				
22	C4	944	47	54				
23	D4	949	61	102	104	109		
24	E4	944	70	108				
25	F4	963	69	116	118			
26	G4	961	60	115				
27	A5	949	56	66	73	74		
28	B5	963	53	55	72			
29	C5	949	46	50	58	57		
30	D5	944	49	51				
31	E5	949	7	12	19	20		
32	F5	032	6	8	14			
33	G5	937	16	24	25	103	105	107
34	A6	032	65	68				
35	F6	944	18					
36	G6	F09	3	4				
37	A7	F09	35	101				
38	B7	F09	37	38				
39	C7	D09	29	30				
40	D7	F09	31	32				
41	E7	F09	39	40				
42	F7	963	5	15	21			
43	G7	F09	11	23				
44	A8	F09	43	44				
45	B8	F09	41	42				
46	C8	F09	33	34				
47	D8	F09	13	26				
48	E8	F09	27	36				
49	F8	F09	22	28				
50	G8	F09	17	125				

TYPE	VCC	GRD
930-963	14	7
SN-7401	4	11
F01-F03	4	11
F09	4	11

LBD - SCHEMATIC REF. GATE NO. CONVERSION

LBD	SCH
1-99	1-99
A0-A9	100-109
B0-B9	110-119
C0-C9	120-129
D0-D9	130-139
E0-E9	140-149
F0-F9	150-159
G0-G9	160-169
H0-H9	170-179
I0-I9	180-189
J0-J9	190-199

Figure 1-2-16. Clock Module Schematic Diagram (Sheet 1 of 2)

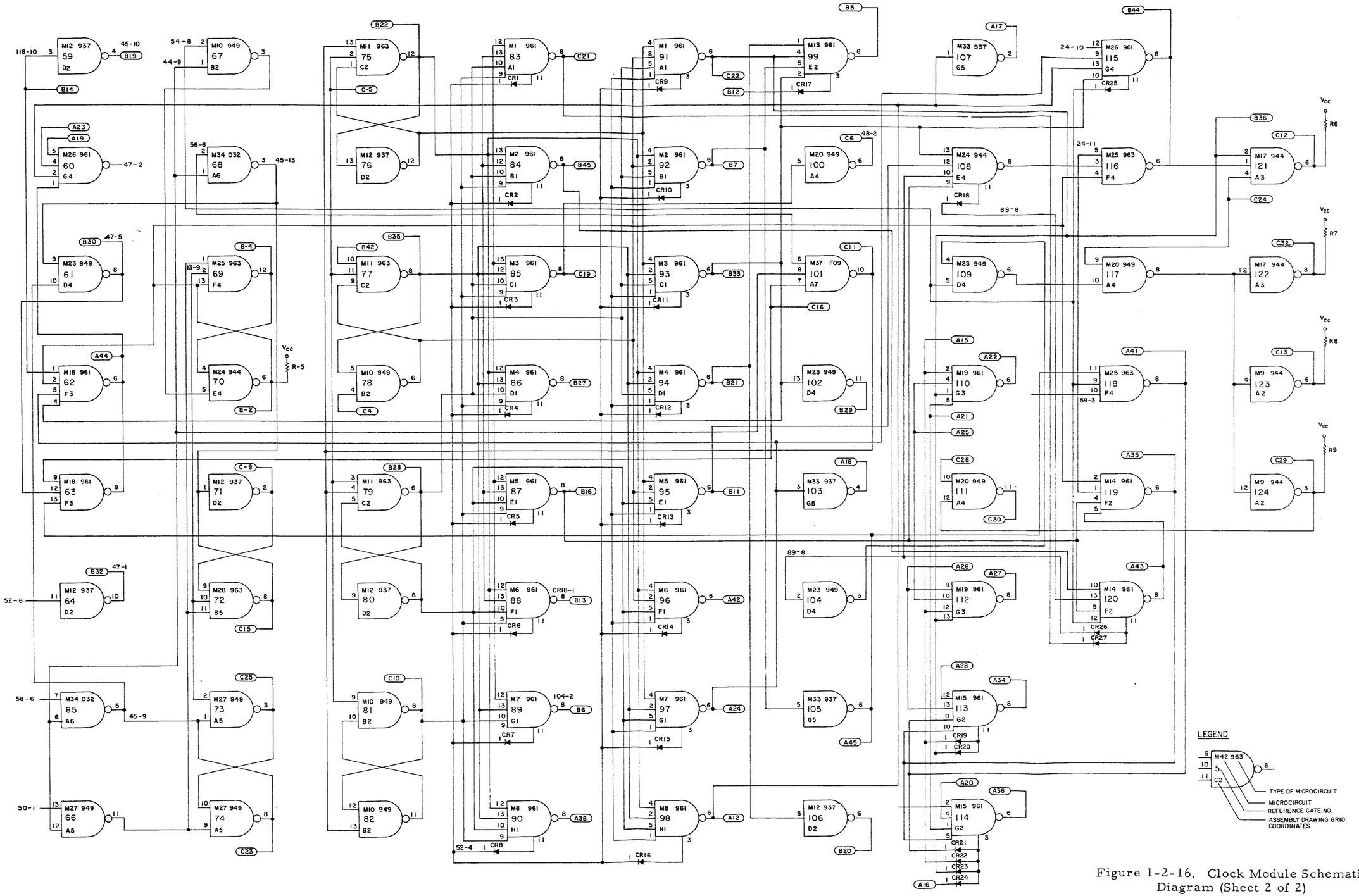
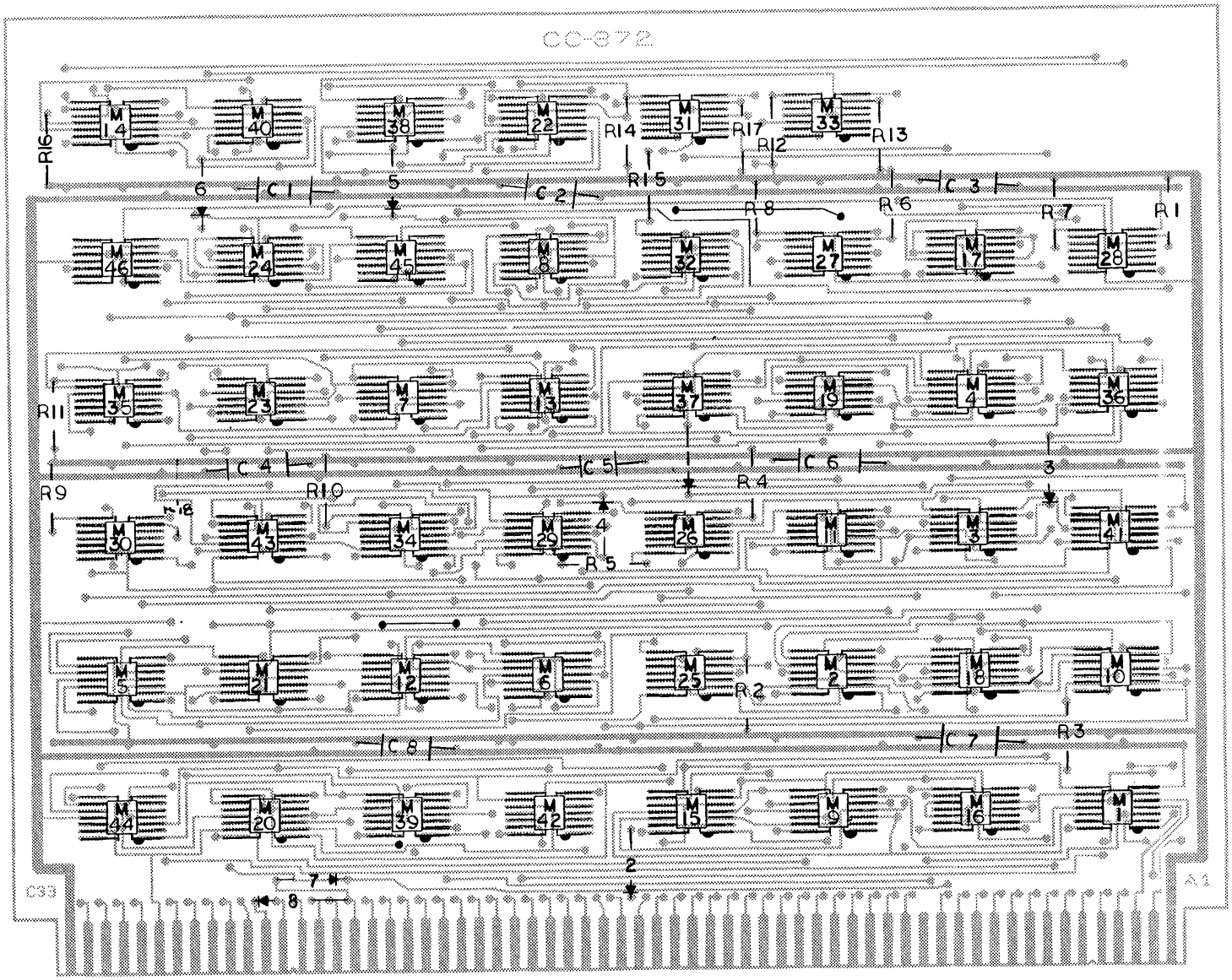


Figure 1-2-16. Clock Module Schematic Diagram (Sheet 2 of 2)

REGULATOR COUNTER MODULE, MODEL CC-372

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C8	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
CR1-CR8	DIODE: Replacement type 1N914	70 943 083 002
M1, M3-M8	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70 950 105 012
M2, M15-M24	MICROCIRCUIT: 949, quad NAND gate integrated circuit	70 950 105 010
M9-M14	MICROCIRCUIT: 937, hex inverter integrated circuit	70 950 105 011
M25-M35	MICROCIRCUIT: 944, power amplifier integrated circuit	70 950 105 008
M36-M40, M42	MICROCIRCUIT: 961, dual NAND gate integrated circuit	70 950 105 009
M41, M43	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M44-M46	MICROCIRCUIT: F-04, flip-flop integrated circuit	70 950 100 004
R1, R2, R6-R14, R16-R18	RESISTOR, FIXED, FILM: 2K ±2%, 1/4W	70 932 114 056
R3, R4, R5	RESISTOR, FIXED, FILM: 510 ohms ±2%, 1/4W	70 932 114 042
R15	RESISTOR, FIXED, FILM: 1K ±2%, 1/4W	70 932 114 049



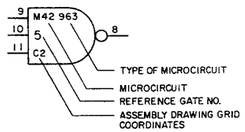
COMPONENT VIEW

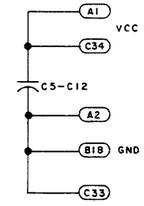
Figure 1-2-17. Regulator Counter Module Parts Location

M NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6
1	H6	963	1	4	6			
2	F5	963	19	20	31			
3	G4	963	38	45	47			
4	G3	963	51	55	59			
5	A5	963	70	71	77			
6	D5	963	86	89	142			
7	C3	963	92	95				
8	D2	963	98	109				
9	F6	937	5	9	11	13	15	
10	H5	937	23	24	26	28	33	34
11	F4	937	35	36	44	46	57	
12	C5	937	82	83	115	124	87	
13	D3	937	99	100	102	112	116	143
14	A1	937	110	130	131	138	144	146
15	E6	949	10	12	14	16		
16	G6	949	2	3	7	63		
17	G2	949	25	27	29	30		
18	G5	949	17	18	32	39		
19	F3	949	50	53	54	61		
20	B6	949	65	66	73	81		
21	B5	949	78	79	93	103		
22	D1	949	108	118				
23	B3	949	120	121	123	129		
24	B2	949	134	135	140	141		
25	E5	944	21	22				
26	E4	944	37	40				
27	F2	944	60	64				
28	H2	944	62	8				
29	D4	944	85	94				
30	A4	944	74	104				
31	E1	944	114	145				
32	E2	944	101	126				
33	F1	944	111	113				
34	C4	944	88	96				
35	A3	944	106	139				
36	H3	961	49	52				
37	E3	961	48	56				
38	C1	961	91	105				
39	C6	961	68	69				
40	B1	961	122	137				
41	H4	032	41	42	43	58		
42	D6	961	67					
43	B4	032	43	84				
44	A6	F04	75					
45	C2	F04	132					
46	A2	F04	127					

TYPE	VCC	GRD
930-963	14	7
SN-7401	4	11
F01-F04	4	11

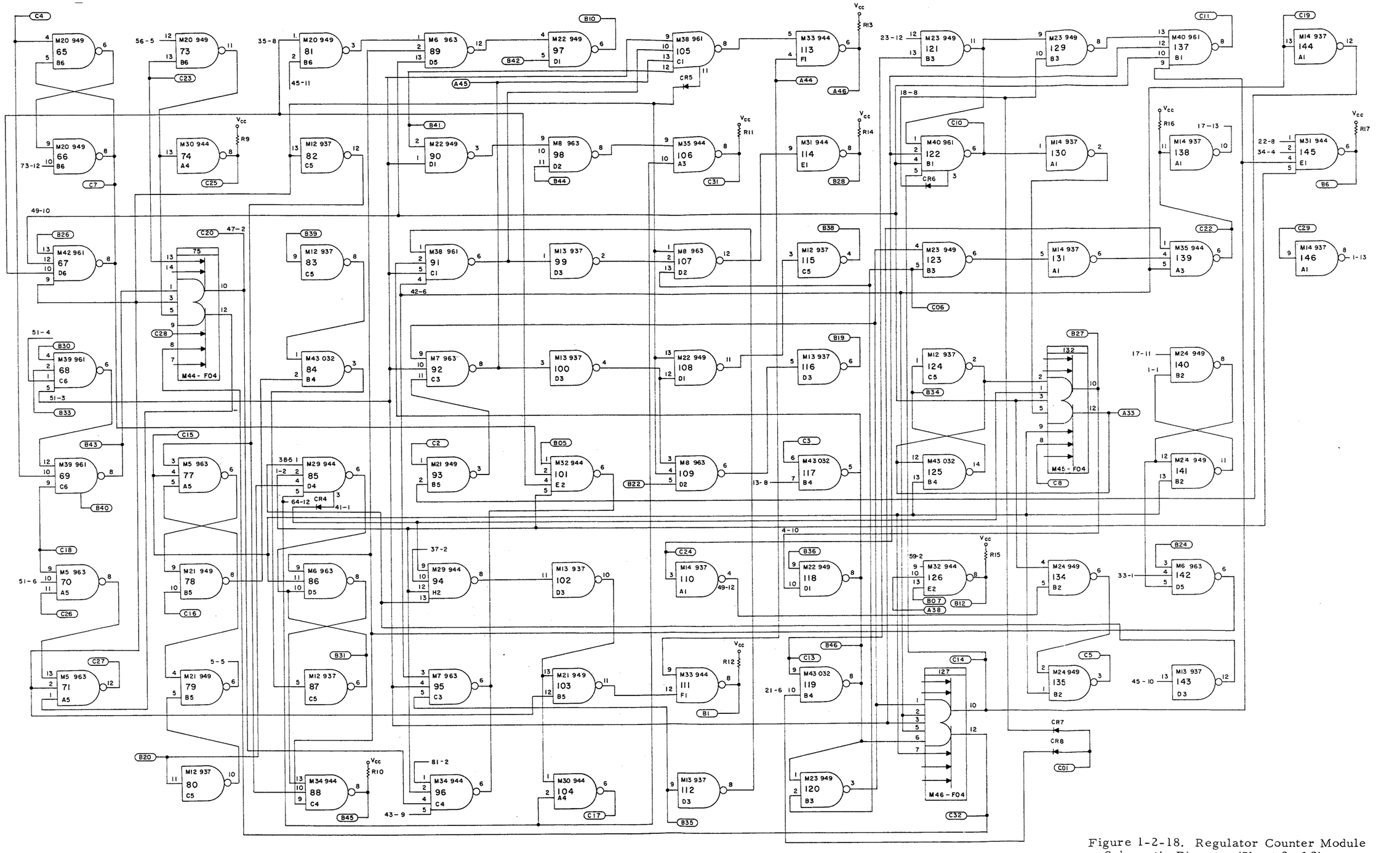
LEGEND





D5651

Figure 1-2-18. Regulator Counter Module Schematic Diagram (Sheet 1 of 2)



D5671

Figure 1-2-18. Regulator Counter Module Schematic Diagram (Sheet 2 of 2)

MEMORY TIMING MODULE, MODEL CC-373

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C32	CAPACITOR, FIXED, MICA DIELECTRIC: 120 μF ±2%, 100 Vdc	70 930 004 219
C33-C40	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
M1, M2, M9 M10, M11	MICROCIRCUIT: 949, quad NAND gate integrated circuit	70 950 105 010
M3, M5, M8 M19, M27	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70 950 105 012
M4, M7, M14 M22, M24-M26	MICROCIRCUIT: 961, dual NAND gate integrated circuit	70 950 105 009
M6, M15, M16	MICROCIRCUIT: 937, fast hex inverter integrated circuit	70 950 105 011
M12, M13, M17, M18, M20, M21 M23	MICROCIRCUIT: 944, power amplifier integrated circuit	70 950 105 008
M28-M36	MICROCIRCUIT: F-03 power amplifier integrated circuit	70 950 100 003
CR1-CR8, CR11	DIODE: Replacement type 1N914	70 943 083 002
CR9, CR10	DIODE	70 943 088 001
Q1	TRANSISTOR, SILICON, NPN: Replacement type 2N3011	70 943 722 001
Q2	TRANSISTOR, SILICON, PNP: Replacement type 2N3012	70 943 721 001
DL1-DL4	DELAY LINE	70 000 206 703
R1-R4, R10, R18	RESISTOR, FIXED, COMPOSITION: 510 ohms ±5%, 1/4W	70 932 007 042
R5, R7, R8	RESISTOR, FIXED, COMPOSITION: 1K ohms ±5%, 1/4W	70 932 007 049
R9	RESISTOR, FIXED, COMPOSITION: 820 ohms ±5%, 1/4W	70 932 007 047
R11	RESISTOR, FIXED, COMPOSITION: 100 ohms ±5%, 1/4W	70 932 007 025
R12	RESISTOR, FIXED, COMPOSITION: 750 ohms ±5%, 1/4W	70 943 007 046

Electrical Parts List (Cont)

Ref. Desig.	Description	Part No.
R13	RESISTOR, FIXED, COMPOSITION: 39 ohms ±5%, 1/2W	70 932 004 015
R14-R16	RESISTOR, FIXED, COMPOSITION: 330 ohms ±5%, 1/4W	70 932 007 037
R17	RESISTOR, FIXED, COMPOSITION: 180 ohms ±5%, 1/2W	70 932 004 031

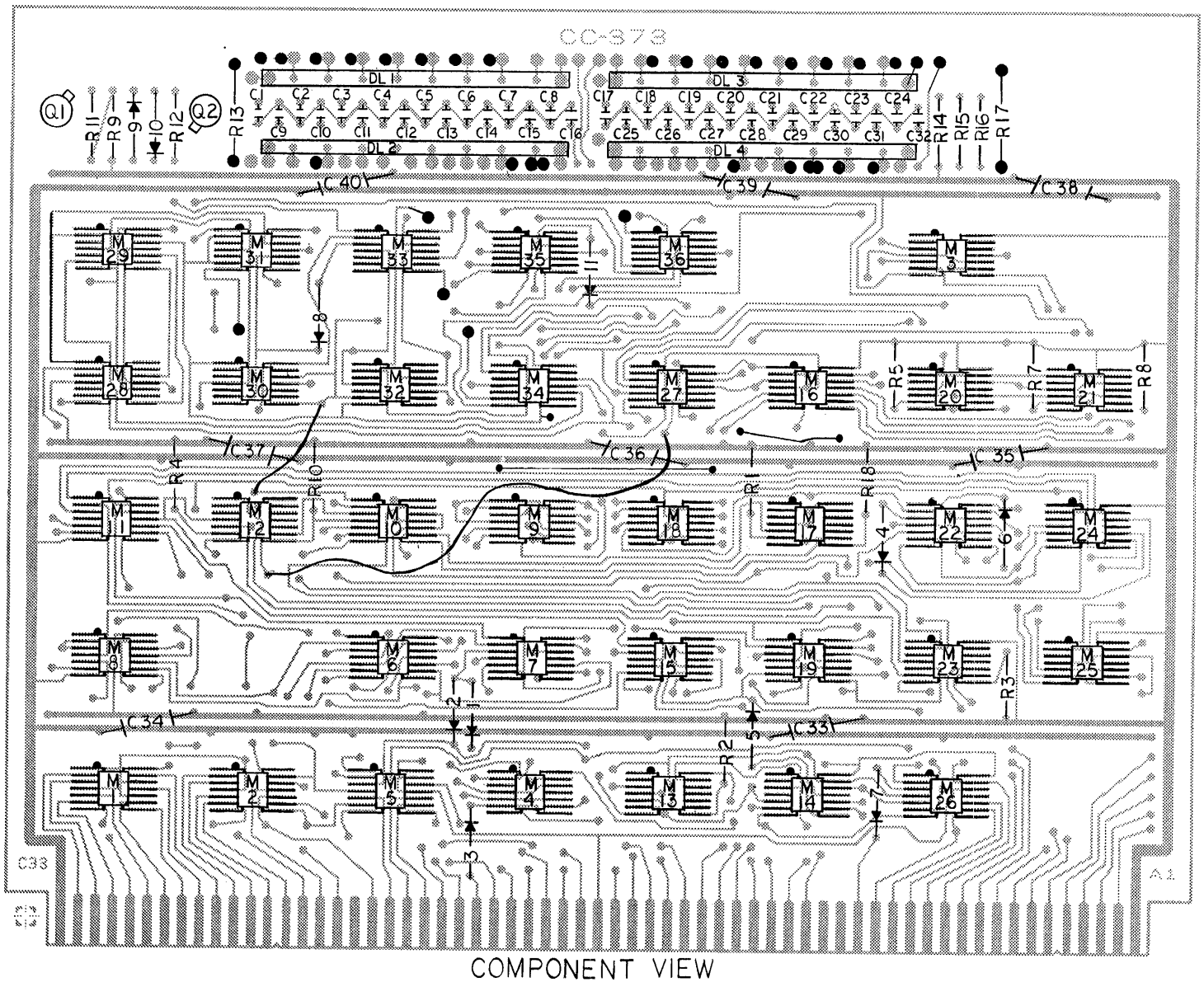


Figure 1-2-19. Memory Timing Module Parts Location

The following temporary jumpers must be inserted prior to the start of any tests.

a. CC-373

Connect P3 to T30
P5 to T40
P1 to T25
P6 to T15
P7 to T13
P8 to T33
P9 to T35
P10 to T12
P11 to T14
P12 to T12
P13 to T2
P14 to T30
P17 to T35
P5 to P15

b. CC-899

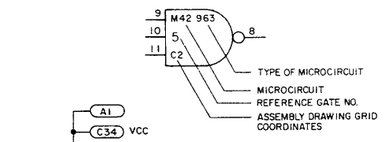
Connect P3 to T23
P5 to T40
P7 to T13
P8 to T33
P9 to T36
P10 to T14
P11 to T14
P12 to T8
P13 to T1
P14 to T30
P15 to T40
P17 to T38
P18 to T13
P6 to T14
P1 to T22

M. NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6
1	A5	949	22	23	29	30		
2	B5	949	21	36	37	51		
3	G1	963	52	53				
4	D5	961	15	16				
5	C5	963	9	28	63			
6	C4	937	8	27	50	72	74	76
7	D4	961	1	71				
8	A4	963	6	7	73			
9	D3	949	67	68	69	70		
10	C3	949	5	35	66	97		
11	A3	949	11	48	99	43		
12	B3	944	55	98				
13	E5	944	13	40				
14	F5	961	20	33				
15	E4	937	14	19	41	49	75	77
16	F2	937	24	25	38	44	56	58
17	F3	944	34	42				
18	E3	944	2	65				
19	F4	963	4	12	26			
20	G2	944	59	60				
21	H2	944	61	62				
22	G3	961	17	39				
23	G4	944	3	54				
24	H3	961	10	18				
25	H4	961	31	32				
26	G5	961	47	57				
27	E2	963	45	46	64			
28	A2	F03	78	85				
29	A1	F03	79	83				
30	B2	F03	86	87				
31	B1	F03	80	81				
32	C2	F03	82	88				
33	C1	F03	89	90				
34	D2	F03	92	93				
35	D1	F03	91	94				
36	E1	F03	95	96				

CC-273 Sheet 1

TYPE	VCC	GRD
930-963	14	7
SN-7401	4	11
F01-F04	4	11

LEGEND



LBD – SCHEMATIC REF. GATE NO. CONVERSION	
LBD	SCH
1-99	1-99
A0-A9	100-109
B0-B9	110-119
C0-C9	120-129
D0-D9	130-139
E0-E9	140-149
F0-F9	150-159
G0-G9	160-169
H0-H9	170-179
I0-I9	180-189
J0-J9	190-199

D5674

Figure 1-2-20. Memory Timing Module Schematic Diagram (Sheet 1 of 2)

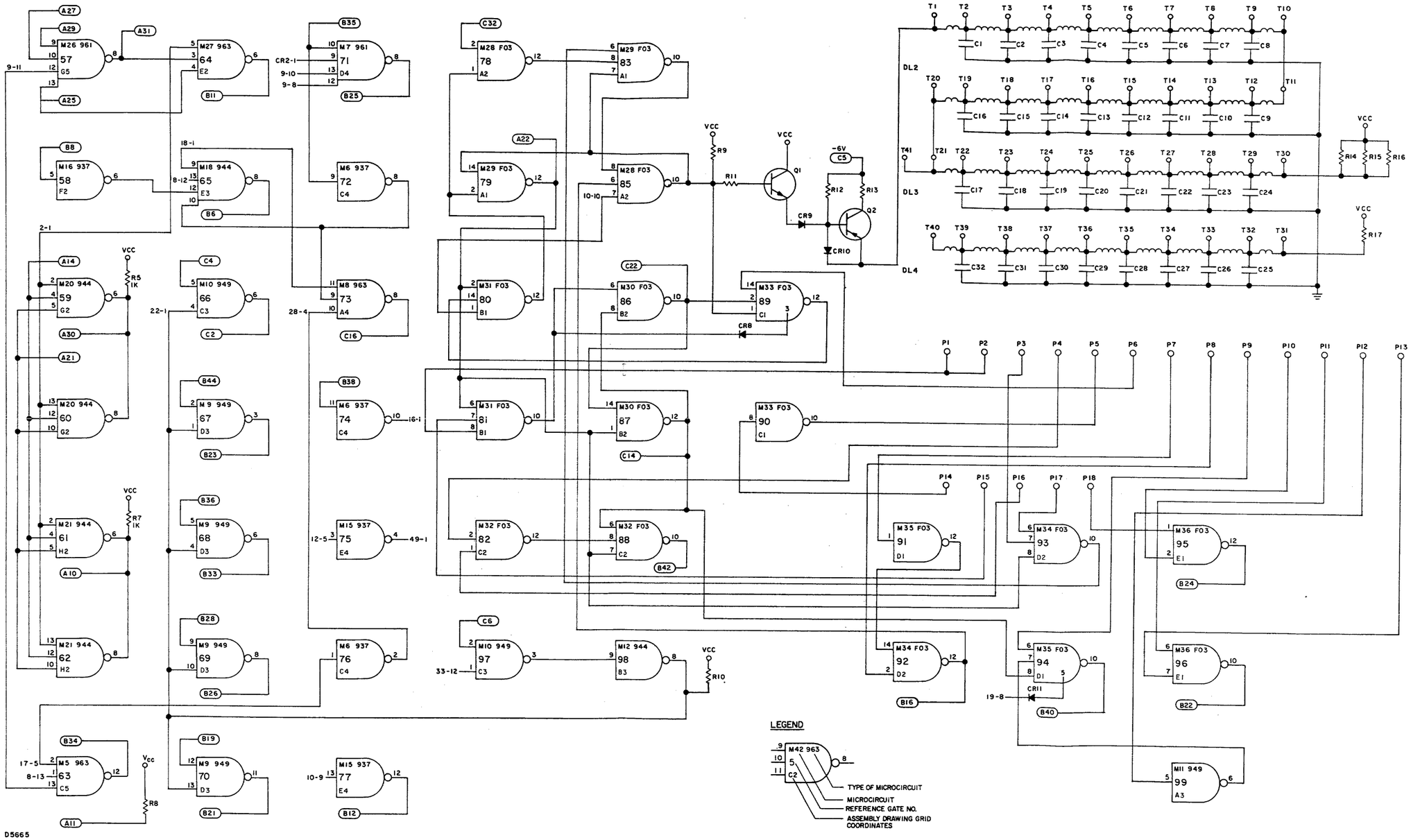


Figure 1-2-20. Memory Timing Module Schematic Diagram (Sheet 2 of 2)

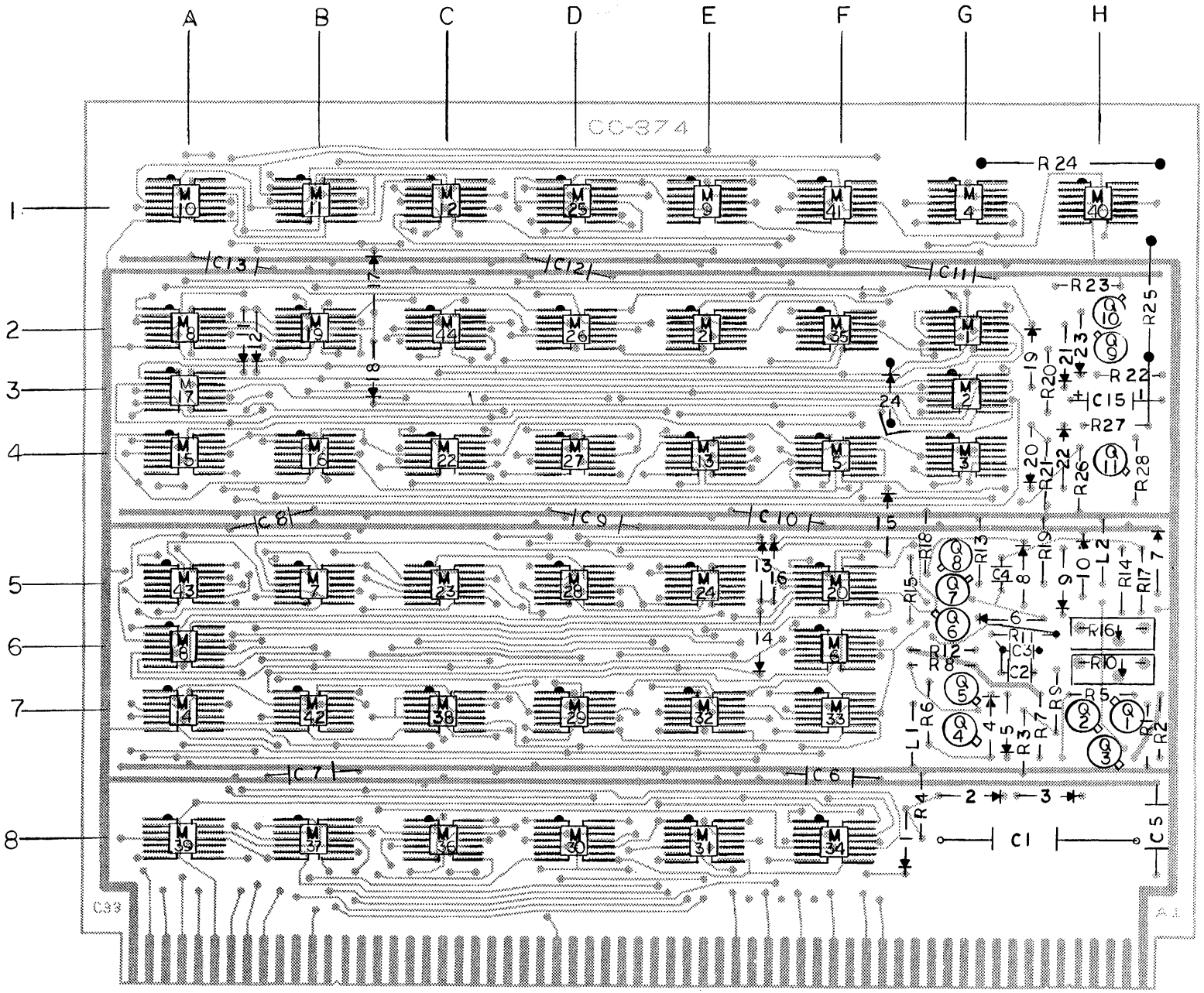
ASR INTERFACE MODULE, MODEL CC-374

Electrical Parts List

Ref. Desig.	Description	Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 1 μF ±5%, 50 Vdc	70 930 316 037
C2	CAPACITOR, FIXED, MICA DIELECTRIC: 300 pF ±5%, 100 Vdc	70 930 011 239
C3	CAPACITOR, FIXED, MICA DIELECTRIC: 10 pF ±5%, 100 Vdc	70 930 011 105
C4	CAPACITOR, FIXED, MICA DIELECTRIC: 680 pF ±5%, 100 Vdc	70 930 011 049
C5-C13	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
C15	CAPACITOR, FIXED, ELECTROLYTIC-TANTALUM: 1 μF ±10%, 35 Vdc	70 930 217 054
CR1-CR6, CR8-CR24	DIODE: Replacement type 1N914	70 943 083 002
CR7	DIODE: Replacement type FD777	70 943 088 001
L1, L2	COIL, R. F: 6.8 μH ±10%	70 939 207 023
M1, M10, M11, M17, M36, M43	MICROCIRCUIT: 962, triple NAND gate integrated circuit	70 950 105 006
M2, M12, M14, M18, M44	MICROCIRCUIT: 936, hex inverter integrated circuit	70 950 105 004
M3, M4, M6, M8, M9, M15, M16, M21, M26-M35, M41	MICROCIRCUIT: F-04, flip-flop integrated circuit	70 950 100 004
M5, M13, M25, M37, M38, M42	MICROCIRCUIT: 946, quad NAND gate integrated circuit	70 950 105 002
M7, M19, M20	MICROCIRCUIT: 930, dual NAND gate integrated circuit	70 950 105 001
M22, M23	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M24	MICROCIRCUIT: 944, power amplifier integrated circuit	70 950 105 008
M39, M40	MICROCIRCUIT: F-03, power amplifier integrated circuit	70 950 100 003

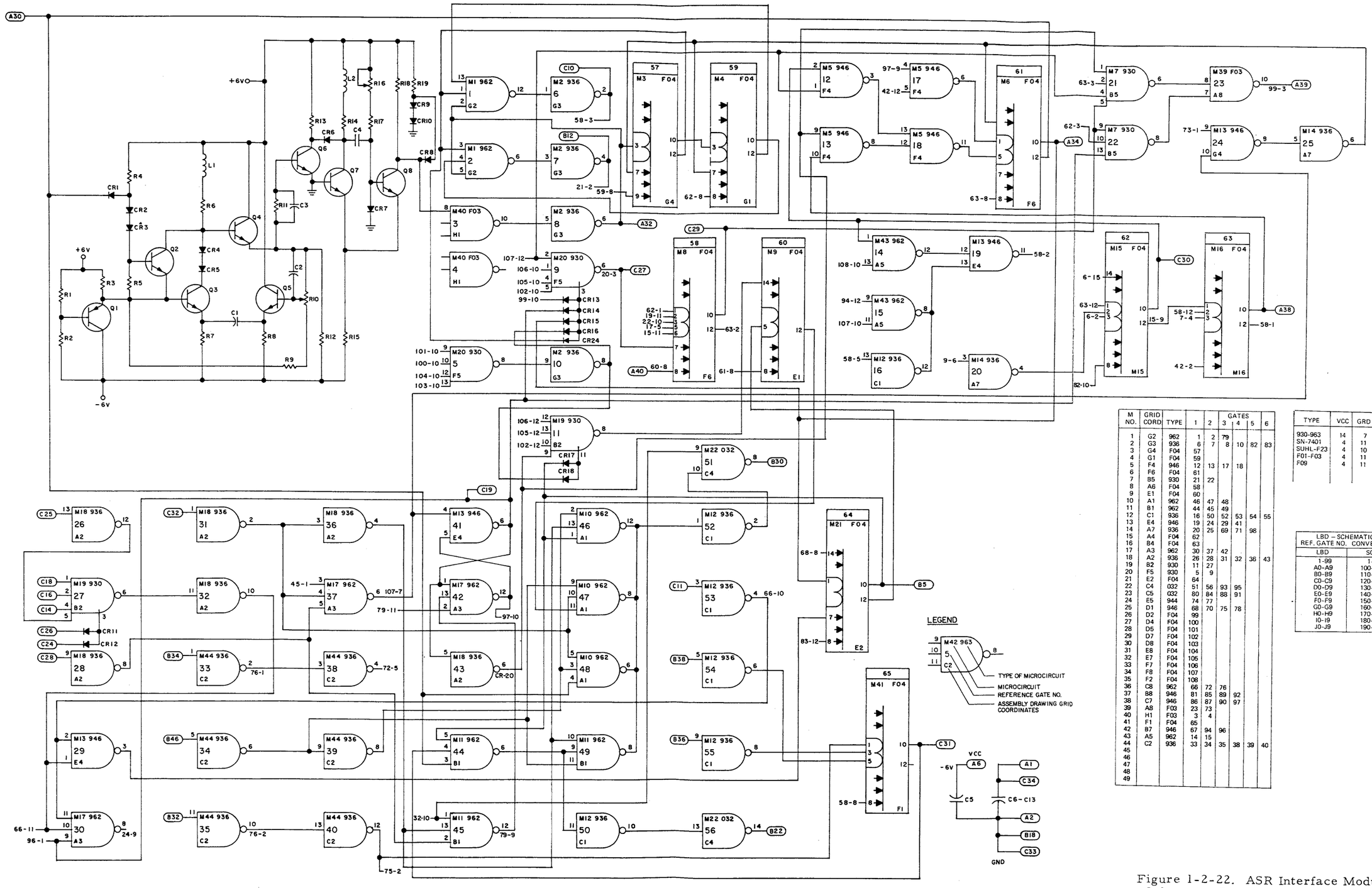
Electrical Parts List (Cont)

Ref. Desig.	Description	Part No.
Q1	TRANSISTOR, SILICON, PNP: Replacement type 2N3012	70 943 721 002
Q2-Q8, Q11	TRANSISTOR, SILICON, NPN: Replacement type 2N3011	70 943 754 002
Q9, Q10	TRANSISTOR, SILICON, NPN: Replacement type 2N2369	70 943 720 001
R1, R3, R5, R12, R13, R18, R23, R26, R28	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4W	70 932 007 049
R2	RESISTOR, FIXED, COMPOSITION: 750 ohms ±5%, 1/4W	70 932 007 046
R4, R6, R11	RESISTOR, FIXED, COMPOSITION: 1.5K ±5%, 1/4W	70 932 007 053
R7, R8	RESISTOR, FIXED, FILM: 2.2K ±2%, 1/4W	70 932 114 057
R9, R17	RESISTOR, FIXED, FILM: 1.5K ±2%, 1/4W	70 932 114 053
R10	RESISTOR, VARIABLE, FILM: 1K ±10%	70 933 302 007
R14	RESISTOR, FIXED, FILM: 1K ±2%, 1/4W	70 932 114 049
R15	RESISTOR, FIXED, FILM: 360 ohms ±2%, 1/4W	70 932 114 038
R16	RESISTOR, VARIABLE, FILM: 10K ±10%	70 933 302 010
R19	RESISTOR, FIXED, COMPOSITION: 270 ohms ±5%, 1/4W	70 932 007 035
R20, R21	RESISTOR, FIXED, COMPOSITION: 2K ±5%, 1/4W	70 932 007 056
R22	RESISTOR, FIXED, COMPOSITION: 4.7K ±5%, 1/4W	70 932 007 065
R24	RESISTOR, FIXED, FILM: 220 ohms ±2, 1 W	70 932 115 033
R25	RESISTOR, FIXED, FILM: 180 ohms ±2%, 1W	70 932 115 031
R27	RESISTOR, FIXED, COMPOSITION: 9.1K ±5%, 1/4W	70 932 007 072



COMPONENT VIEW

Figure 1-2-21. ASR Interface Module Parts Location



M NO.	GRID CORD	TYPE	GATES 1	2	3	4	5	6
1	G2	962	1	2	79			
2	G3	936	6	7	8	10	82	83
3	G4	F04	57					
4	G1	F04	59					
5	F4	946	12	13	17	18		
6	F6	F04	61					
7	B5	930	21	22				
8	A6	F04	58					
9	E1	F04	60					
10	A1	962	46	47	48			
11	B1	962	44	45	49			
12	C1	936	16	50	52	53	54	55
13	E4	946	19	24	29	41		
14	A7	936	20	25	69	71	98	
15	A4	F04	62					
16	B4	F04	63					
17	A3	962	30	37	42			
18	A2	936	26	28	31	32	36	43
19	B2	930	11	27				
20	F5	930	5	9				
21	E2	F04	64					
22	C4	032	51	56	93	95		
23	C5	032	80	84	88	91		
24	E5	944	74	77				
25	D1	946	68	70	75	78		
26	D2	F04	99					
27	D4	F04	100					
28	D5	F04	101					
29	D7	F04	102					
30	D8	F04	103					
31	E8	F04	104					
32	E7	F04	105					
33	F7	F04	106					
34	F8	F04	107					
35	F2	F04	108					
36	C8	962	66	72	76			
37	B8	946	81	85	89	92		
38	C7	946	86	87	90	97		
39	A8	F03	23	73				
40	H1	F03	3	4				
41	F1	F04	65					
42	B7	946	67	94	96			
43	A5	962	14	15				
44	C2	936	33	34	35	38	39	40
45								
46								
47								
48								
49								

TYPE	VCC	GRD
930-963	14	7
SN-7401	4	11
SUHL-F23	4	10
F01-F03	4	11
F09	4	11

LBD – SCHEMATIC REF. GATE NO. CONVERSION	
LBD	SCH
1-99	1-99
A0-A9	100-109
B0-B9	110-119
C0-C9	120-129
D0-D9	130-139
E0-E9	140-149
F0-F9	150-159
G0-G9	160-169
H0-H9	170-179
I0-I9	180-189
J0-J9	190-199

Figure 1-2-22. ASR Interface Module Schematic Diagram (Sheet 1 of 2)

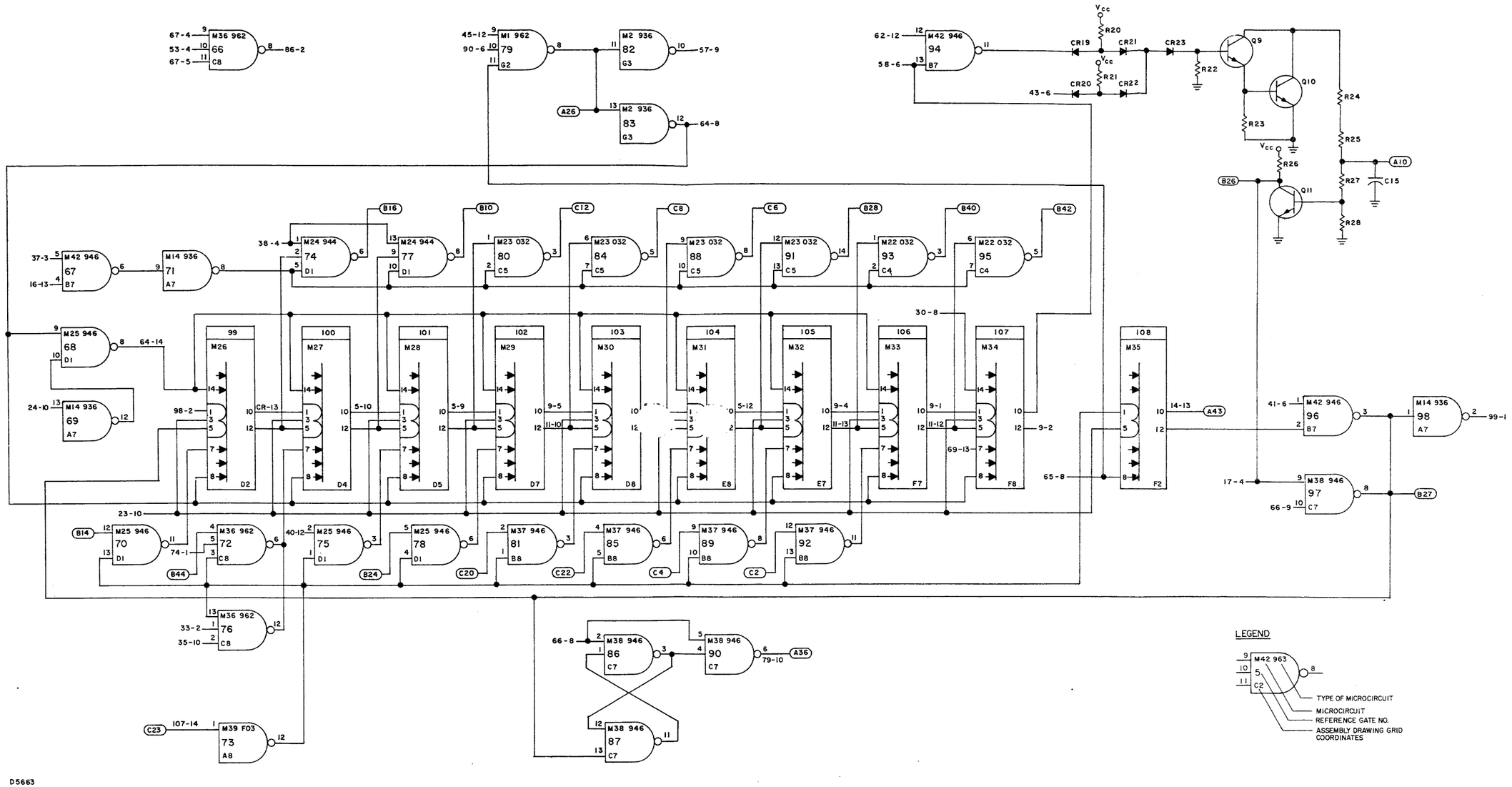


Figure 1-2-22. ASR Interface Module Schematic Diagram (Sheet 2 of 2)

HIGH SPEED A-U NO. 1 MODULE, MODEL CC-375

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C5	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
CR1-CR17	DIODE: Replacement type 1N914	70 943 083 002
M1-M4, M17	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M5, M10, M12, M20-M23, M25	MICROCIRCUIT: 944, power amplifier integrated circuit	70 950 105 008
M6, M9, M14, M15, M24, M26	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70 950 105 012
M7, M18, M19	MICROCIRCUIT: 937, fast hex inverter integrated circuit	70 950 105 011
M8, M13, M29	MICROCIRCUIT: 961, dual NAND gate integrated circuit	70 950 105 009
M11, M16, M27, M28	MICROCIRCUIT: 949, quad NAND gate integrated circuit	70 950 105 010
R1, R2	RESISTOR, FIXED, COMPOSITION: 2K ±5%, 1/4W	70 932 007 056

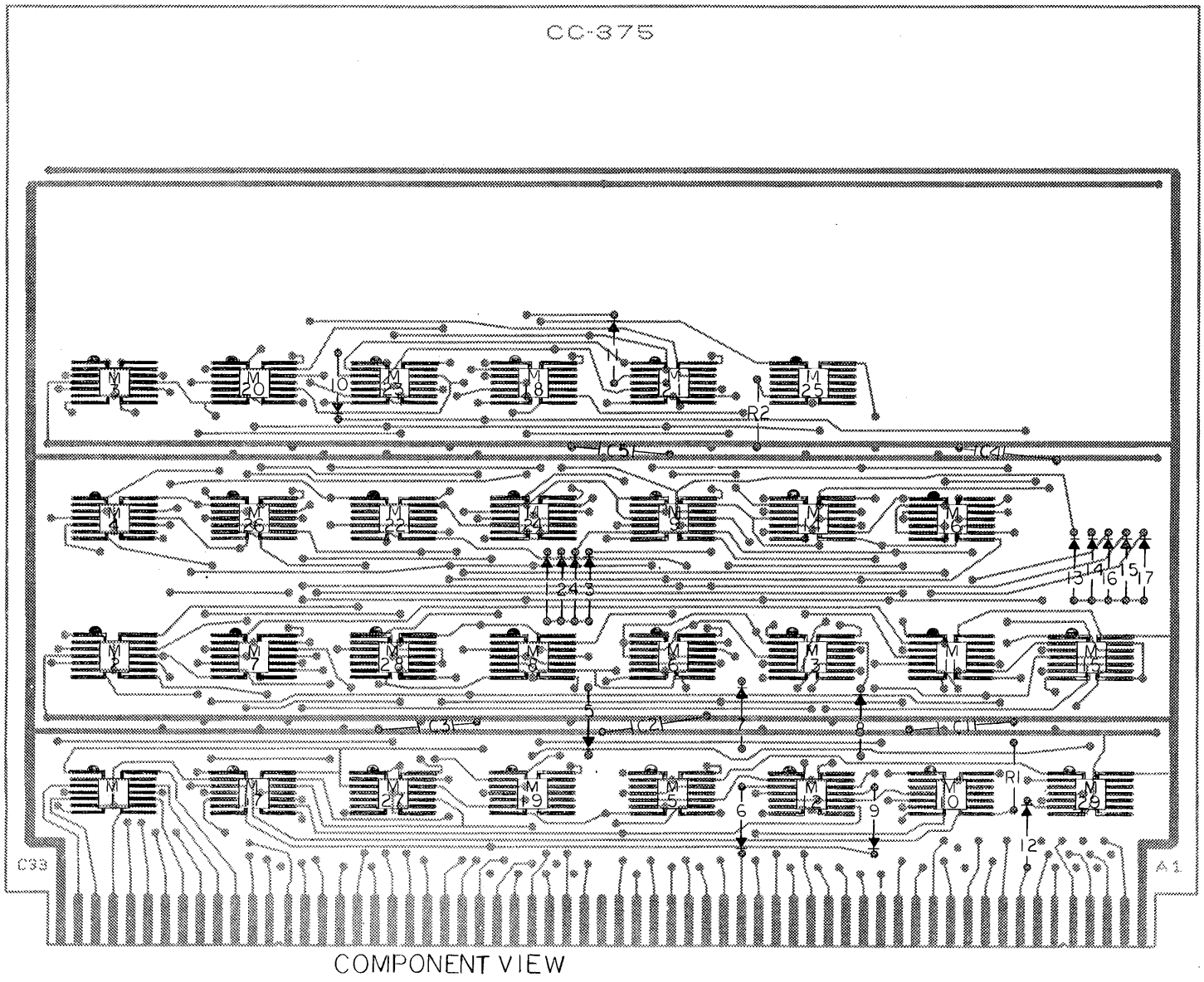


Figure 1-2-23. High Speed A-U No. 1 Module Parts Location

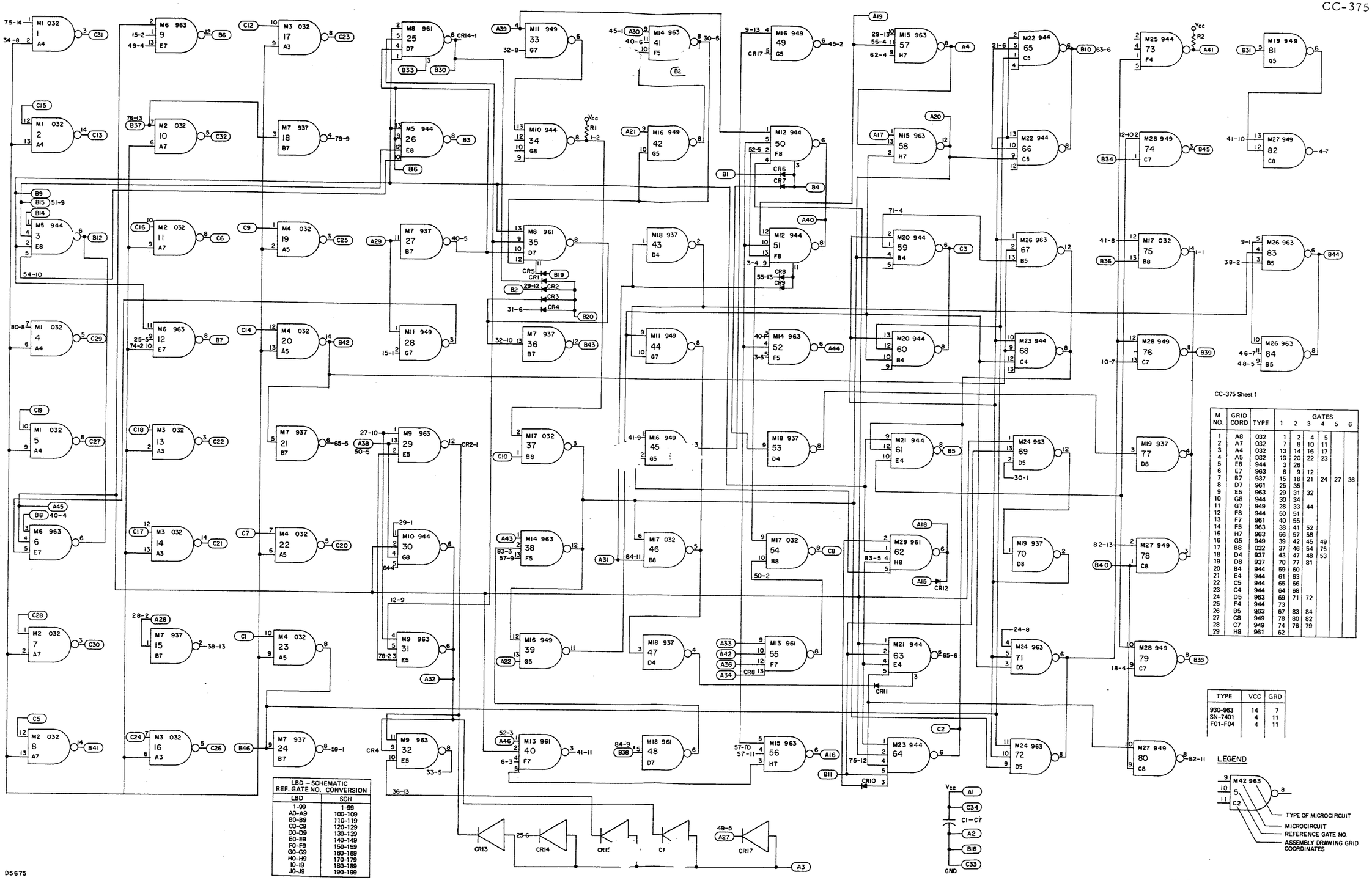


Figure 1-2-24. High Speed A-U No. 1 Module Schematic Diagram

HIGH SPEED A-U NO. 2 MODULE, MODEL CC-401

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C5	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µF ±20%, 50 Vdc	70 930 313 016
CR1-CR14	DIODE: Replacement type 1N914	70 943 083 002
M1-M6	MICROCIRCUIT: 032, quad NAND gate integrated circuit	70 950 100 032
M7, M22, M23	MICROCIRCUIT: 937, fast hex inverter integrated circuit	70 950 105 011
M8-M11, M13, M14, M18	MICROCIRCUIT: 944, power amplifier integrated circuit	70 950 105 008
M12, M21	MICROCIRCUIT: 949, quad NAND gate integrated circuit	70 950 105 010
M15-M17	MICROCIRCUIT: 961, dual NAND gate integrated circuit	70 950 105 009
M19, M20	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70 950 105 012
R1, R2	RESISTOR, FIXED, COMPOSITION: 2K ±5%, 1/4W	70 932 007 056

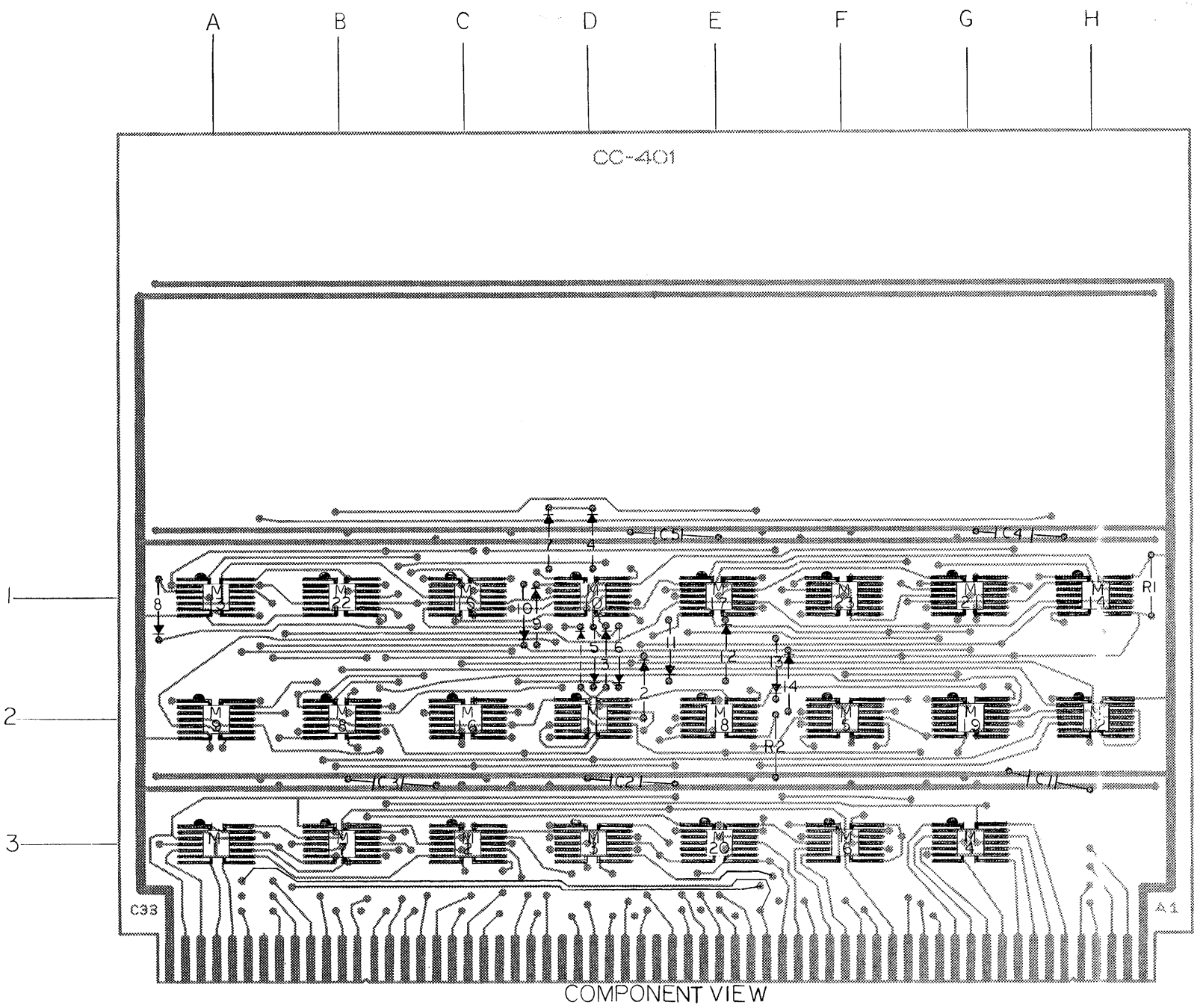


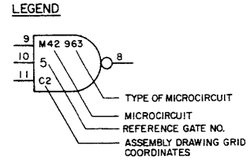
Figure 1-2-25. High Speed A-U No. 2 Module Parts Location

TYPE	VCC	GRD
930-963	14	7
SN-7401	4	11
SUHL-F23	4	10
F01-F03	4	11
F09	4	11

CC-401

M NO.	CRID CORD	TYPE	GATES 1	2	3	4	5	6
1	A8	032	1	2	3	4		
2	C8	032	5	6	7	8		
3	D8	032	9	10	11	12		
4	G8	032	13	14	15	16		
5	F7	032	20	21	22	23		
6	F8	032	28	29	50	58		
7	B8	937	17	18	19	24	30	31
8	B7	944	38	39				
9	A7	944	35	60				
10	D5	944	36	46				
11	D7	944	37	45				
12	H7	949	33	34	42			
13	A5	944	53	54				
14	H5	944	47	59				
15	C5	961	41	52				
16	C7	961	51	61				
17	E5	961	49	62				
18	E7	944	25	65				
19	G7	963	32	66				
20	E8	963	26	55				
21	G5	949	40	56	57	68		
22	B5	937	27	43	44	67		
23	F5	937	48	63	64			

LEGEND



LBD – SCHEMATIC REF. GATE NO. CONVERSION	
LBD	SCH
1-99	1-99
A0-A9	100-109
B0-B9	110-119
C0-C9	120-129
D0-D9	130-139
E0-E9	140-149
F0-F9	150-159
G0-G9	160-169
H0-H9	170-179
I0-I9	180-189
J0-J9	190-199

D5654

Figure 1-2-26. High Speed A-U No. 2 Module Schematic Diagram

EXTENDED ADDRESS MODULE, MODELS CC-510A AND CC-869

Electrical Parts List

Ref. Desig.	Description	Part No.
C1 - C6	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70930313016
CR1 - CR4	DIODE, SILICON	70943083002
M1, M7	MICROCIRCUIT: 937, hex inverter integrated circuit	70950105011
M2, M38	MICROCIRCUIT: 949, quad NAND gate integrated circuit	70950105010
M3, M8, M41	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70950105012
M4, M10	MICROCIRCUIT: 032, NAND gate integrated circuit, Type SN 7401	70950100032
M5, M6, M37*	MICROCIRCUIT: 944, dual NAND gate integrated circuit	70950105008
M9	MICROCIRCUIT: 961, dual NAND gate integrated circuit	70950105009
M11 - M13	MICROCIRCUIT: F-04, flip-flop integrated circuit	70950100004
M14 - M21*	MICROCIRCUIT: F-01, NAND gate integrated circuit	70950100001
M22 - M36, M39*	MICROCIRCUIT: F-03, power amplifier integrated circuit	70950100003
M40	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	70950100002
R1 - R23, R25 - R31, R34, R35*	RESISTOR, FIXED, COMPOSITION: 62 ohms ±5%, 1/4W	70932007020
R24, R32, R33, R36*	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4W	70932007049

*Model CC-869 does not use M14 - M37, M39, and R1 - R36.

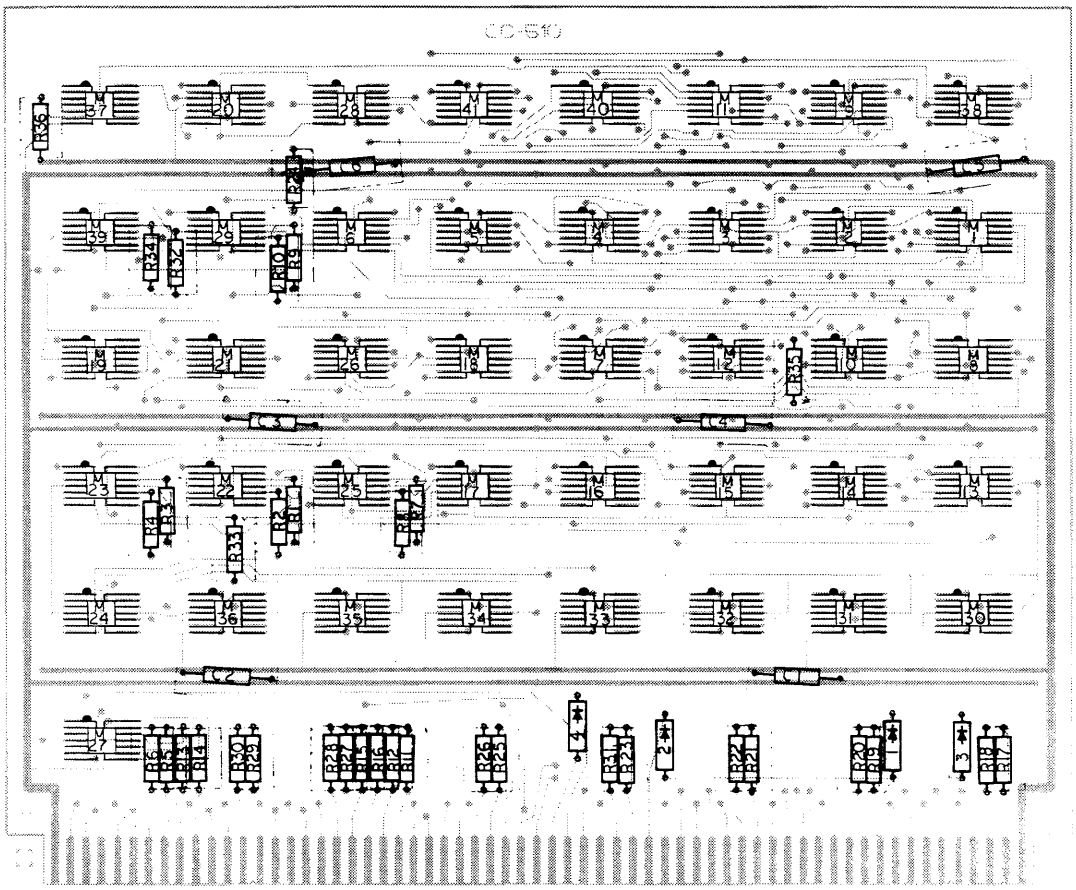


Figure 1-2-27. Extended Address Module, Model CC-510A
(Drawing No. C70025464702, Rev C)

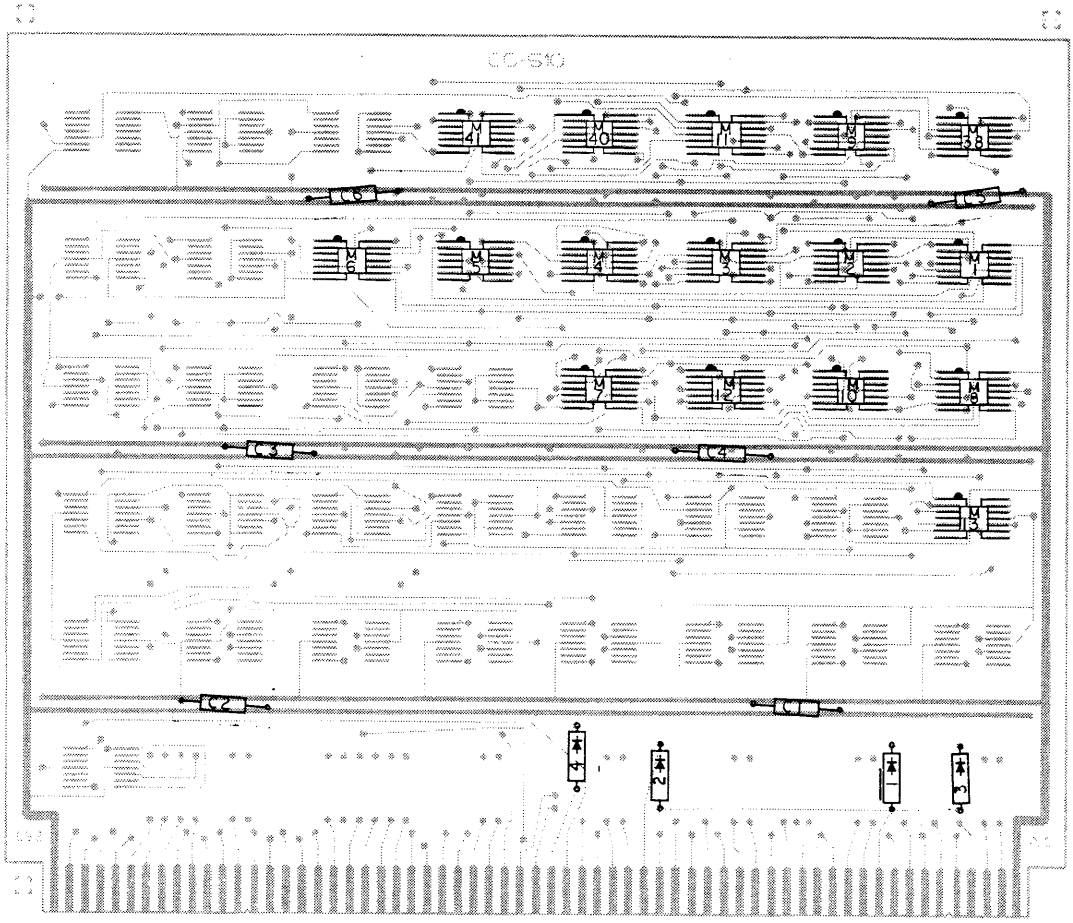


Figure 1-2-28. Extended Address Module, Model CC-869
(Drawing No. C 70025464703, Rev C)

MEMORY PARITY BOARD, MODELS CC-558 AND CC-621

Electrical Parts List

Ref. Desig.	Description	Part No.
C1 - C8*	CAPACITOR, FIXED, PLASTIC: 0.033 μF ±20%, 50 Vdc	70930313016
CR1 - CR7*	DIODE, SILICON	70943083002
M1 - M4*	MICROCIRCUIT: 949, quad NAND gate integrated circuit	70950105010
M5 - M7*	MICROCIRCUIT: 963, triple NAND gate integrated circuit	70950105012
M8 - M12*	MICROCIRCUIT: 961, dual NAND gate integrated circuit	70950105009
M13 - M18*	MICROCIRCUIT: 032, NAND gate integrated circuit, Type SN 7401	70950100032
M19 - M22*	MICROCIRCUIT: 937, hex inverter integrated circuit	70950105011
M23, M24	MICROCIRCUIT: F-03, power amplifier integrated circuit	70950100003
M25 - M34*	MICROCIRCUIT: F-04, flip-flop integrated circuit	70950100004
M35	MICROCIRCUIT: F-02, NAND gate integrated circuit	70950100002
R1, R2*	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4W	70932007049

*Model CC-621 does not use C1, C4, C7, CR1 - CR7, M3, M4, M7, M9 - M17, M19 - M22, M25 - M34, R1, R2.

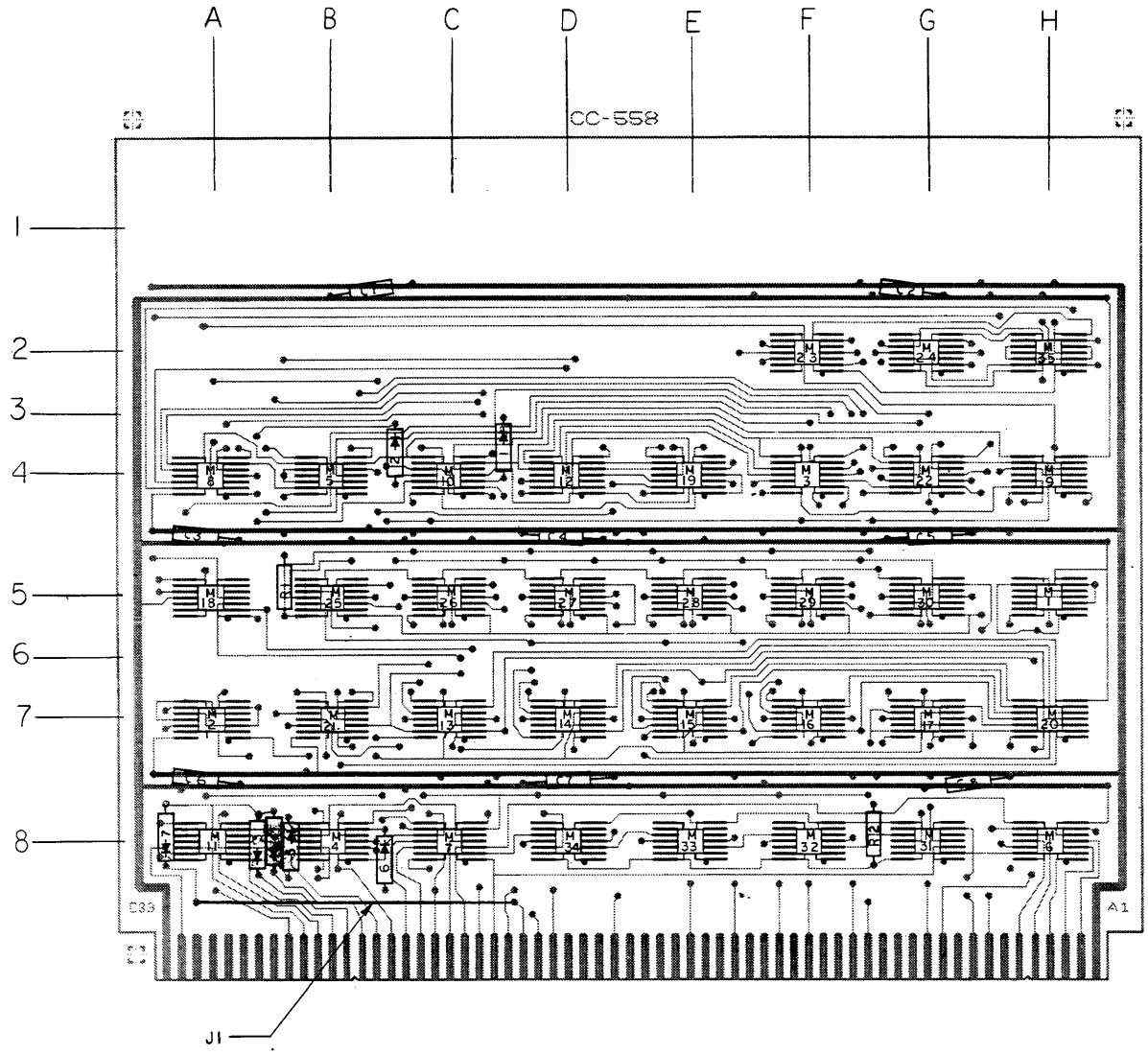
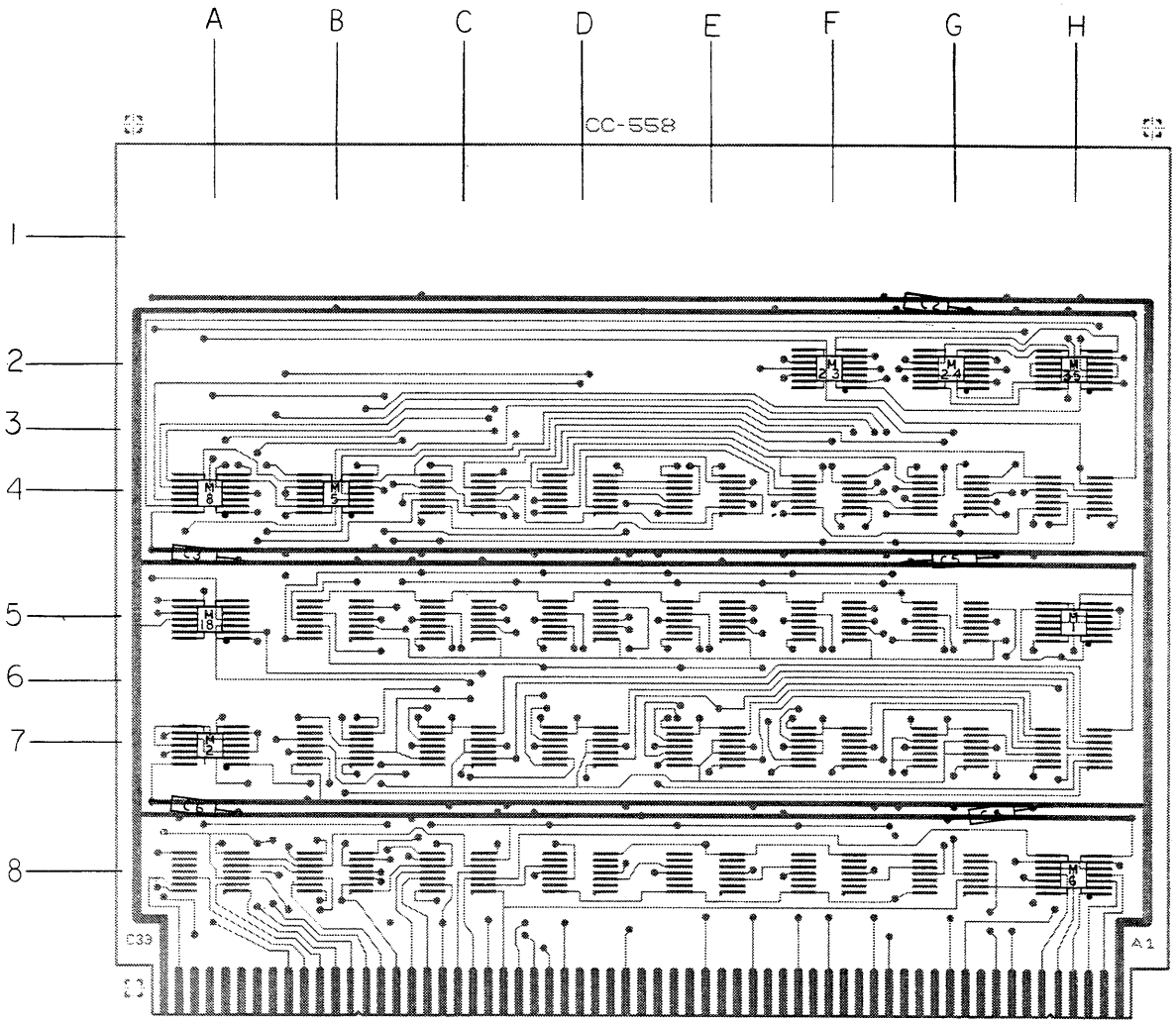


Figure 1-2-29. Memory Parity Board, Model CC-558
(Drawing No. C 70025966701, Rev B)



COMP VIEW

Figure 1-2-30. Memory Parity Board, Model CC-621
(Drawing No. C 70025966702, Rev B)

CABLE PAC, MODEL CC-672

The Cable PAC, Model CC-672 (Figures 1-2-31 and 1-2-32), contains 16 1K resistors and one 2.2 μF capacitor. One side of each component is connected to +6V. The other side of each component is connected to individual plated-through holes and connector pins. In addition, 16 plated-through holes (numbers 18-31) are connected directly to 16 connector pins (numbers 51-66). All plated-through holes can accept No. 24 AWG wire.

Model CC-672
Electrical Parts List

Ref. Desig.	Description	Part No.
C1	CAPACITOR, FIXED, ELECTROLYTIC: 2.2 μF ±20%, 35 Vdc	70930217017
J1, J2	WIRE, TINNED: No. 24 AWG	70940001020
R1-R16	RESISTOR, FIXED, COMPOSITION: 1K ± 5%, 1/4W	70932007049
--	SLEEVING, ELECTRICAL	70981003814

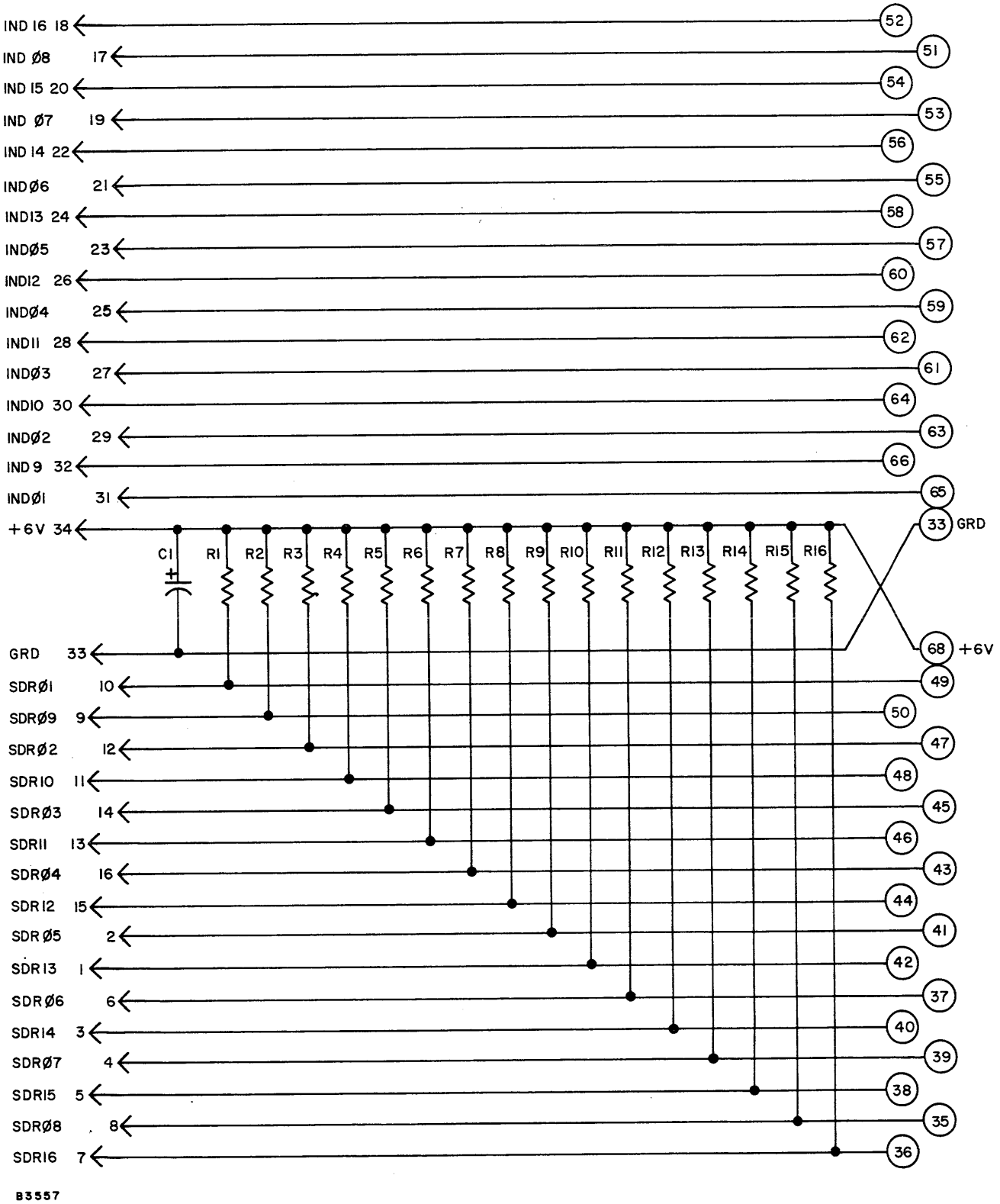


Figure 1-2-31. Cable PAC, Model CC-672, Schematic Diagram

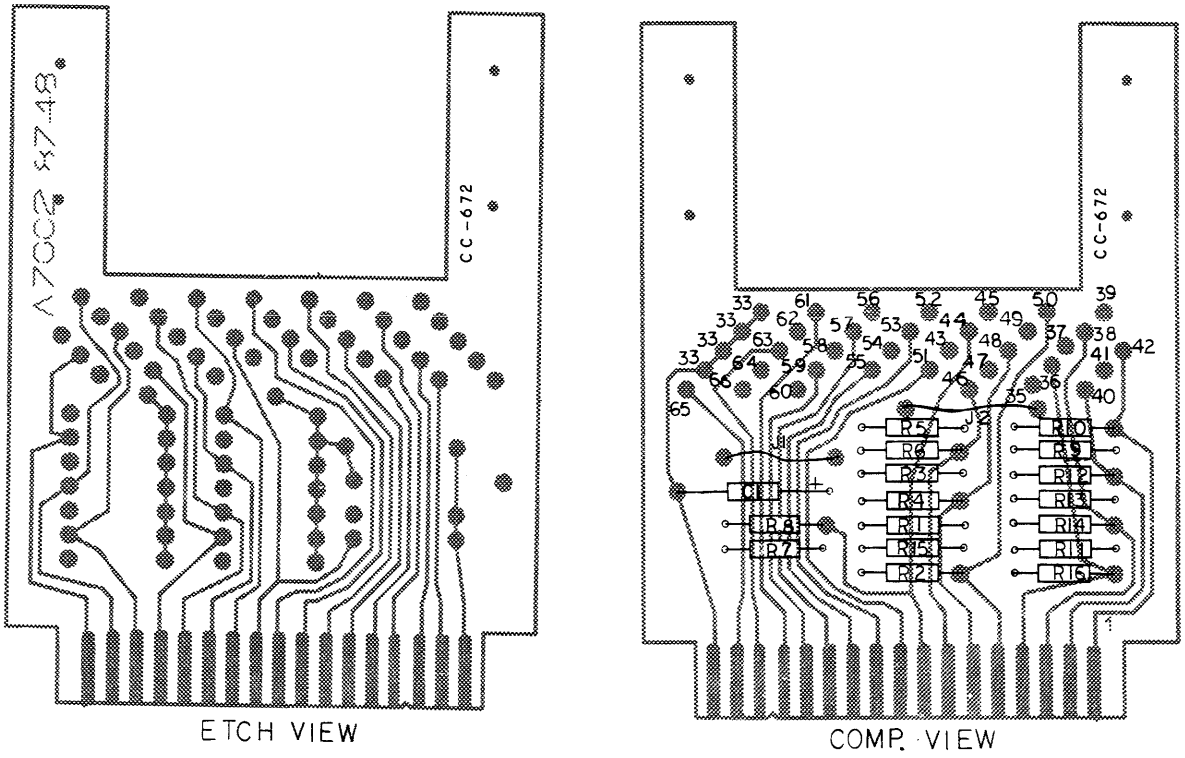


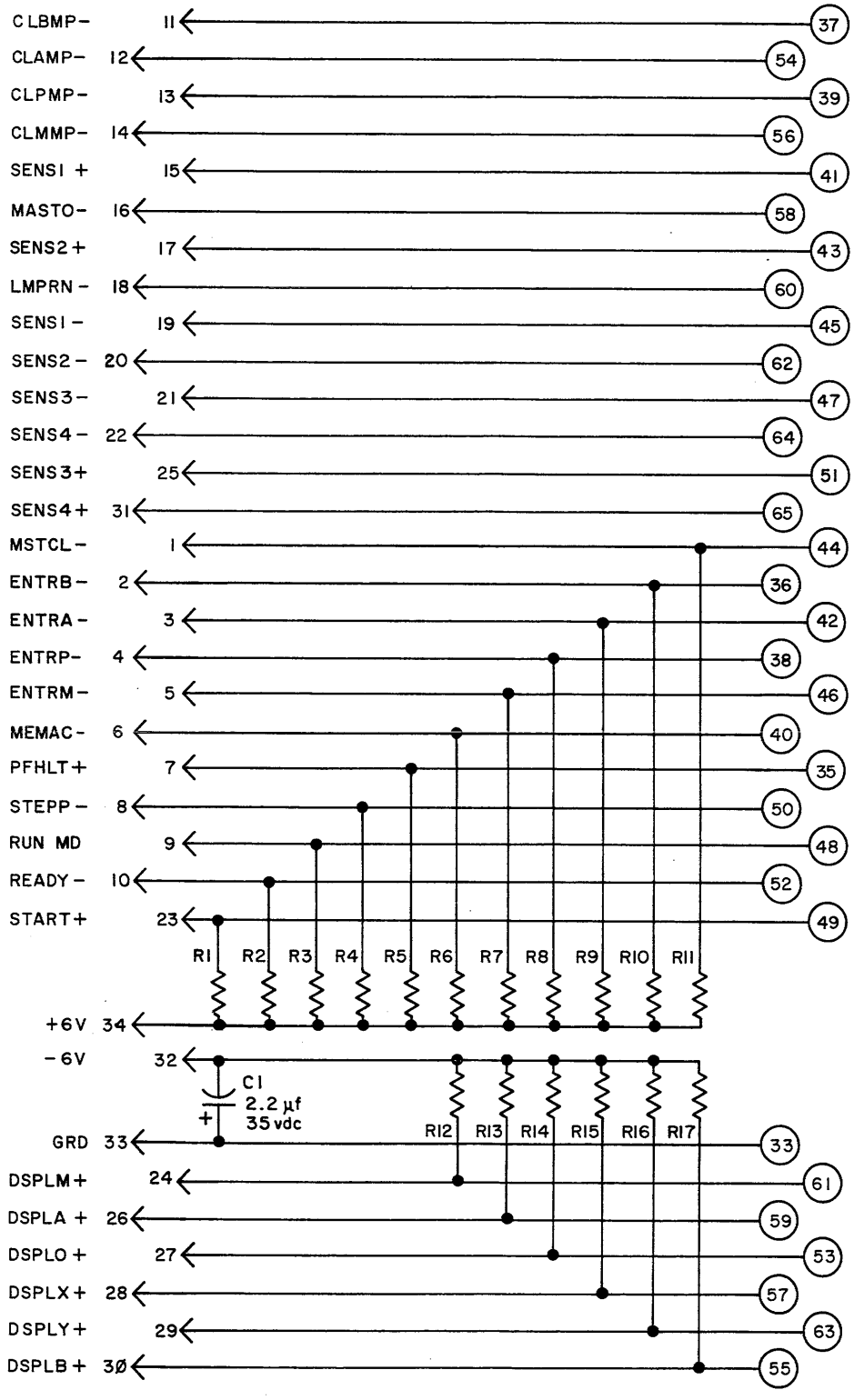
Figure 1-2-32. Model CC-672 Parts Location

CABLE PAC, MODEL CC-681

The Cable PAC, Model CC-681 (Figures 1-2-33 and 1-2-34), contains 17 1K resistors and one 2.2 μF capacitor. One side of 11 resistors (R1-R11) is connected to +6V, and six resistors and one capacitor are connected to -6V. The other side of each component is connected to individual plated-through holes and connector pins. In addition, 14 plated-through holes (numbers 11-22, 25, 31) are connected directly to 14 connector pins. All plated-through holes can accept No. 24 AWG wires. This PAC is used with the bottom harness and can be used in the Model 316 ruggedized computer.

Model CC-681
Electrical Parts List

Ref. Desig.	Description	Part No.
C1	CAPACITOR, FIXED, ELECTROLYTIC: 2.2 μF ± 20%, 35 Vdc	70930217017
J1-J3	WIRE, TINNED: No. 24 AWG	70940001020
R1-R17	RESISTOR, FIXED, COMPOSITION: 1K ± 2%, 1/4 W	70932114049
--	SLEEVING, ELECTRICAL	70981003804



A3560

Figure 1-2-33. Cable PAC, Model CC-681, Schematic Diagram

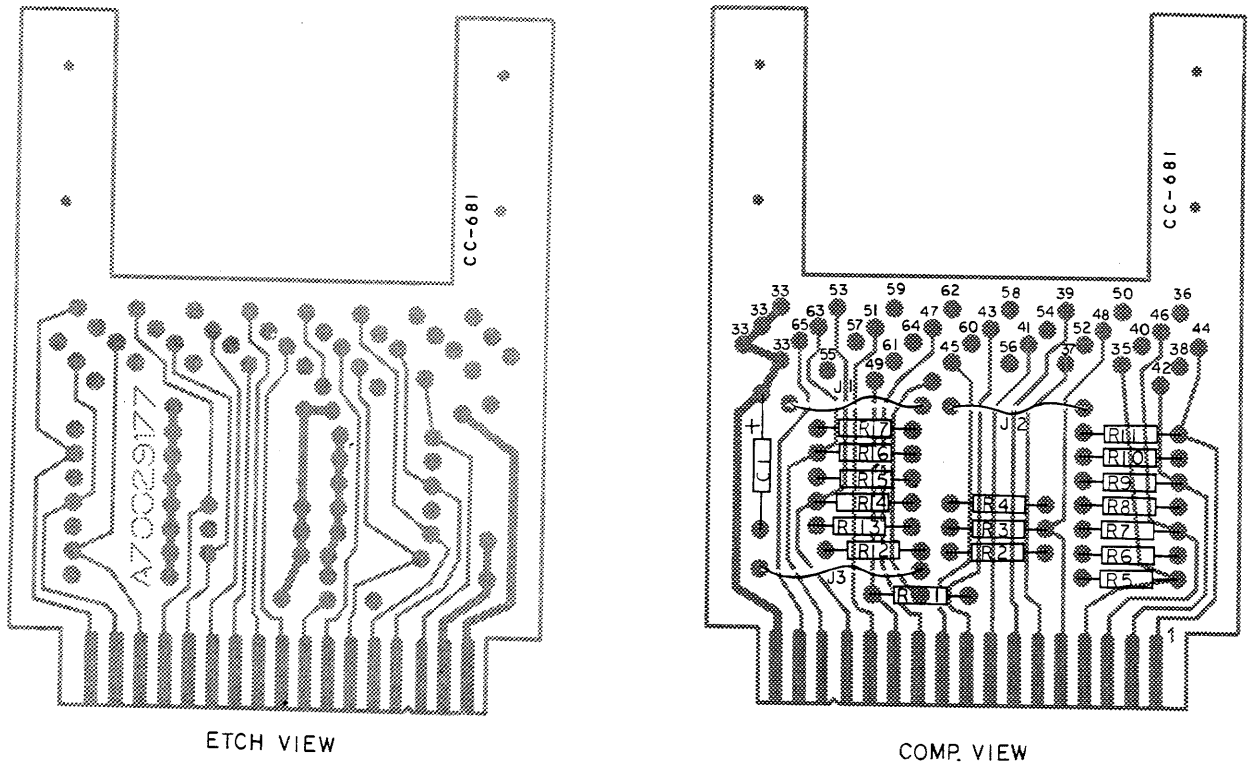


Figure 1-2-34. Model CC-681 Parts Locations

CHAPTER II
CSM-160 CORE MEMORY MODULE

SECTION 1
DESCRIPTION

The CSM-160 Core Memory Module is a high-speed, digital storage device capable of storing a maximum of 16 bits of information in 4096 locations, expandable to 16,384 locations in increments of 4096. Data is stored in an array of 30 mil ferrite cores. Selection of address is accomplished by use of conventional four-wire coincident-current techniques. The switching time of the cores and the frequency characteristics of the driving and logic circuitry permit a full-cycle time of 1.6 μs. The memory does not contain a data register or a timing generator. Memory address signals are received from the address bus at the beginning of any memory operation. The appropriate timing signals are also received and the selection of a location is accomplished in the memory core array. During a memory load (clear-write) cycle, data are supplied to the memory from the computer and stored at the selected address. During a memory-unload (read-regenerate) cycle, the data word at the selected location is first transferred to the computer and then regenerated (rewritten) into the core array.

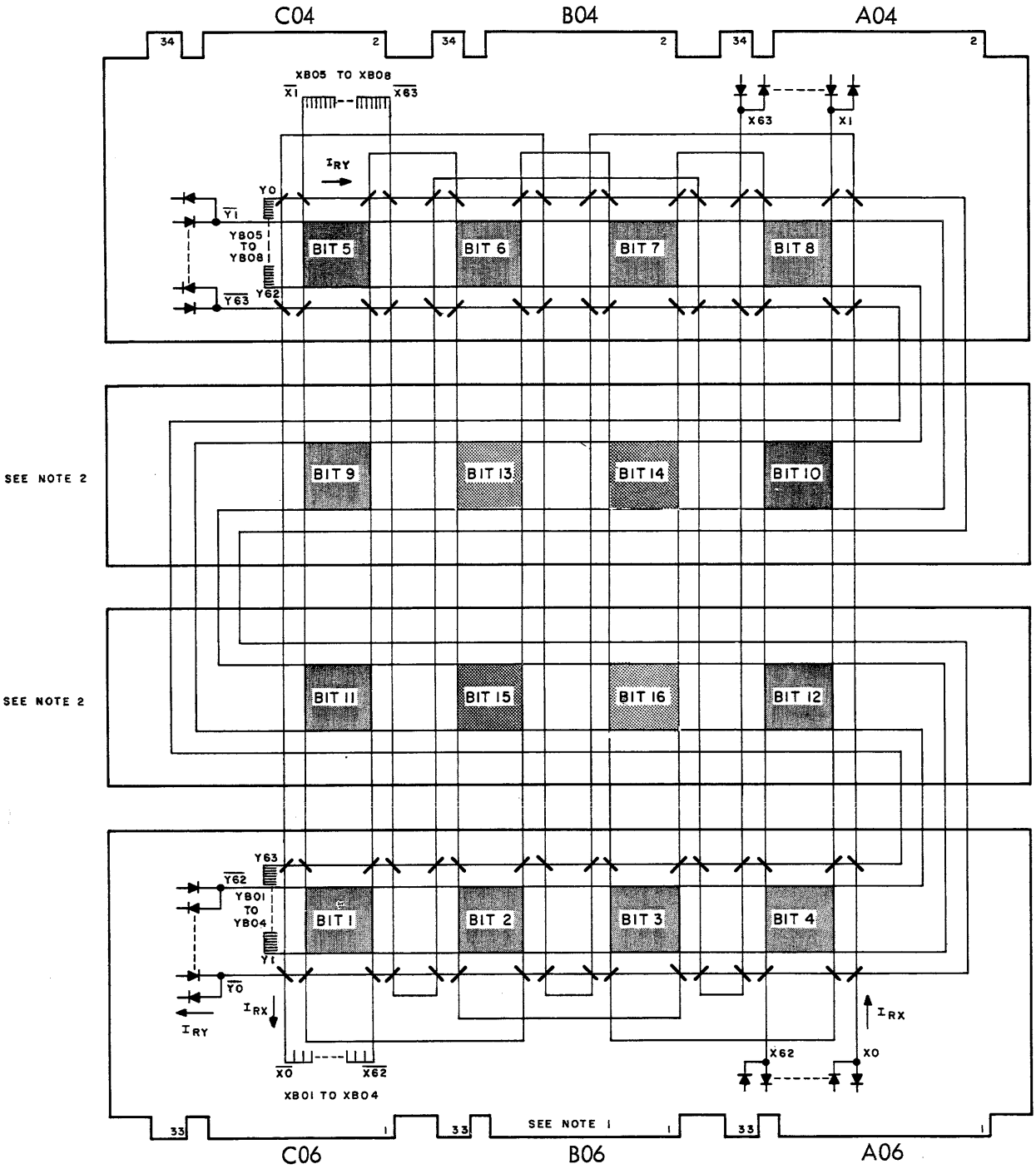
SYSTEM LAYOUT

The system consists of modular connector BLOC assemblies holding groups of μ-PACs. The solderless-wrap connector assembly is a single piece of molded, glass-filled phenolic capable of holding eight μ-PACs. The memory module is contained in three connector assemblies arranged in a 1 x 3 connector plane.

The core stack is a plug-in unit requiring six μ-PAC connectors, three on each side (Figure 2-1-1). The stack assembly is made up of four glass epoxy boards, each containing four core mats of 4096 cores interconnected to make a stack of 16 bit words.

LOGIC SIGNAL LIST

Logic signals used in the memory are identified and defined in Table 2-1-1. Positive signals (+6V) are labeled "+", and ground signals (0V) are labeled "-". Amplified signals have a letter following the polarity indicator (e.g., XXXX+A).



NOTES:

1. VIEWED FROM CORE MAT SIDE.
2. CENTER BOARDS NOT PRESENT FOR AN 8-BIT STACK.
3. X0–X63 & Y0-Y63 ARE DEFINED AS THE CURRENT SOURCE END AT READ TIME. $\overline{X0}$-$\overline{X63}$ & $\overline{Y0}$-$\overline{Y63}$ ARE DEFINED AS THE CURRENT SINK AT READ TIME.

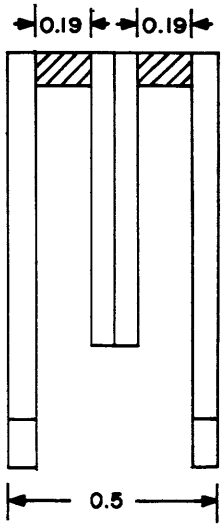


Figure 2-1-1. Stack Coding Diagram

Table 2-1-1
Logic Signal List

Mnemonic	Name
BANK- A through D	Memory Bank Select
INHBX+	Inhibit Command
M01FF+ to M16FF+	Memory Module Data Inputs
MAD05- to MAD16-	Memory Address Inputs
MADCL-	Memory Address Clear Command
MBSYX+	Memory Busy Signal
MEMCI+	Memory Cycle Initiate
MM01F- to MM16F	Sense Amplifier Output Pulses
MSTCL-	Master Clear Pulse
RMBSX-	Reset Memory Busy Pulse
RTDL-	Reset Timing Delay Line Pulse
RZ01+ to RZ16+	Inhibit Winding Termination Resistors
STROB-	Sense Amplifier Strobe
SW01+ tp SW16+	Sense Windings
SWCYX-	Start Write Cycle Pulse
UNSL-	Unit Select Command
UNSL+A through C	Unit Select Signal
WRITE-	Write Enable Signal
XB01+ to XB08+	X-Bus Selection Outputs
XCSR+	X-Current Source Resistor
XD01+ to XD16+	X-Drive Selection Outputs
XRSW-	X-Read Switch Signal
XTIMG+	X-Read/Write Timing
XWSW-	X-Write Switch Signal
XYRE-	X & Y Read Enable Signal
XYWE-	Y-Read Switch Signal X & Y Write Enable Signal
YB01+ to YB08+	Y-Bus Selection Outputs
YCSR+	Y-Current Source Resistor
YD01+ to YD16+	Y-Drive Selection Outputs
YTIMG+	Y-Read/Write Timing
ZW01± to ZW16±	Inhibit Windings

SPECIFICATIONS

Capacity

4K randomly addressable 16-bit words, expandable to 16K in 4K increments.

Storage Mode

Coincident-current magnetic core array (3D, 4-wire)
X0 through X63 X Drive Line
Y0 through Y63 Y Drive Line

Cycle Time

1.6 μs

Input Levels

Positive (Passive): +2.4V to +6.3V
Ground (Active): 0V to 0.5V at 2.0 mA (max)

Output Levels

Positive (Passive): +6.3V max at 0 mA; +3.0V to +5.0V at 0.3 mA
Ground (Active): +0.5V max at 13.6 mA

Memory Cycle Timing

For each cycle, the computer must provide the memory with an address and a read or write indication, and provide the timing circuits (located outside the memory) with a start signal. Once the cycle has been initiated, another cycle cannot be started until 1.6 μs has elapsed. During a read cycle, information will be available no more than the time presented in Figure 2-1-2. If the memory is performing a write cycle, information must be made available to the memory within the time specificied in Figure 2-1-2. Interface connections are shown in Section 4 (LBD 80.06).

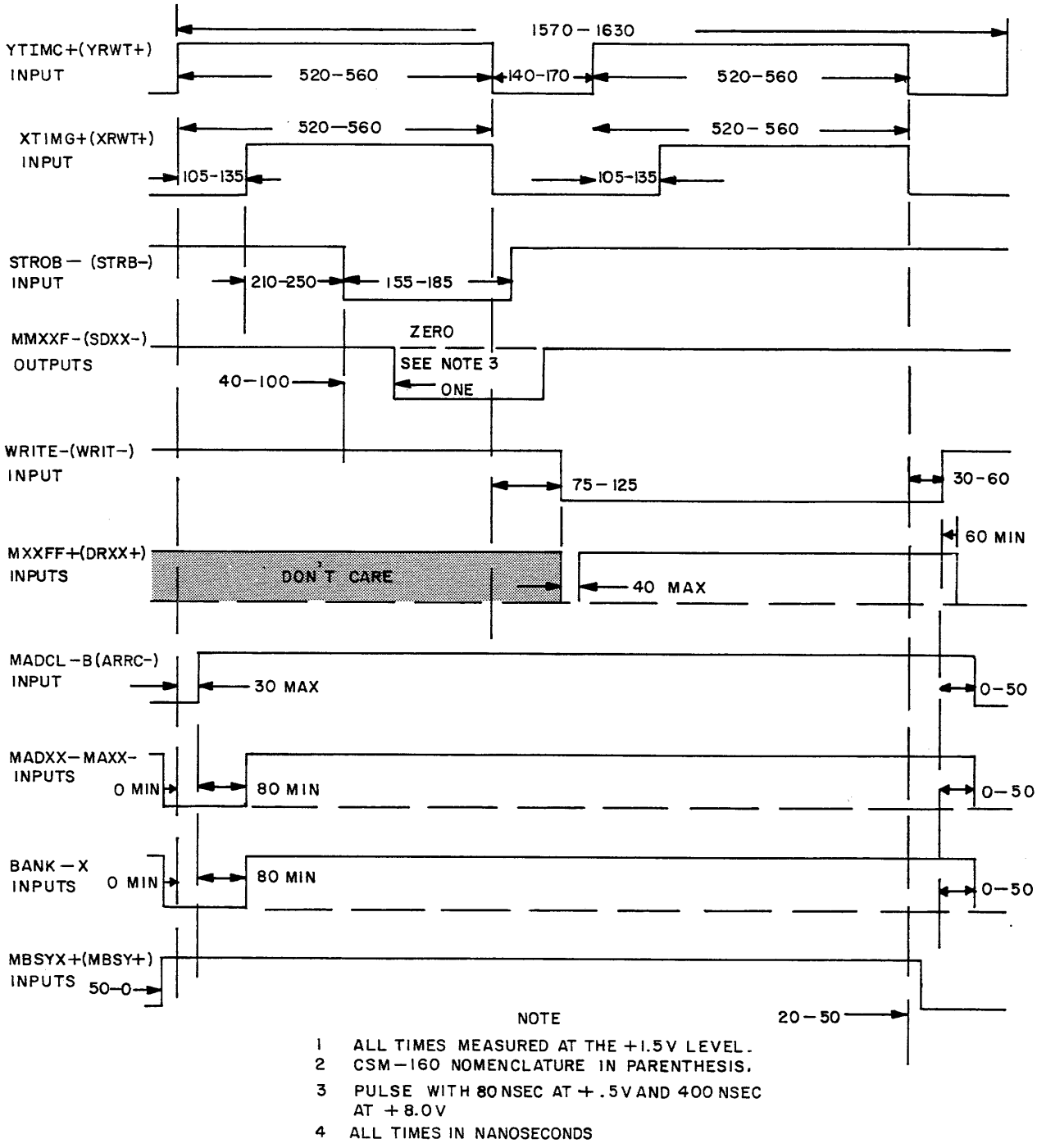


Figure 2-1-2. Interface Timing Requirements for all Units Except A70023577705 (70942507002 Stack) (A70110011397, Rev G)

SECTION 2
PRINCIPLES OF OPERATION

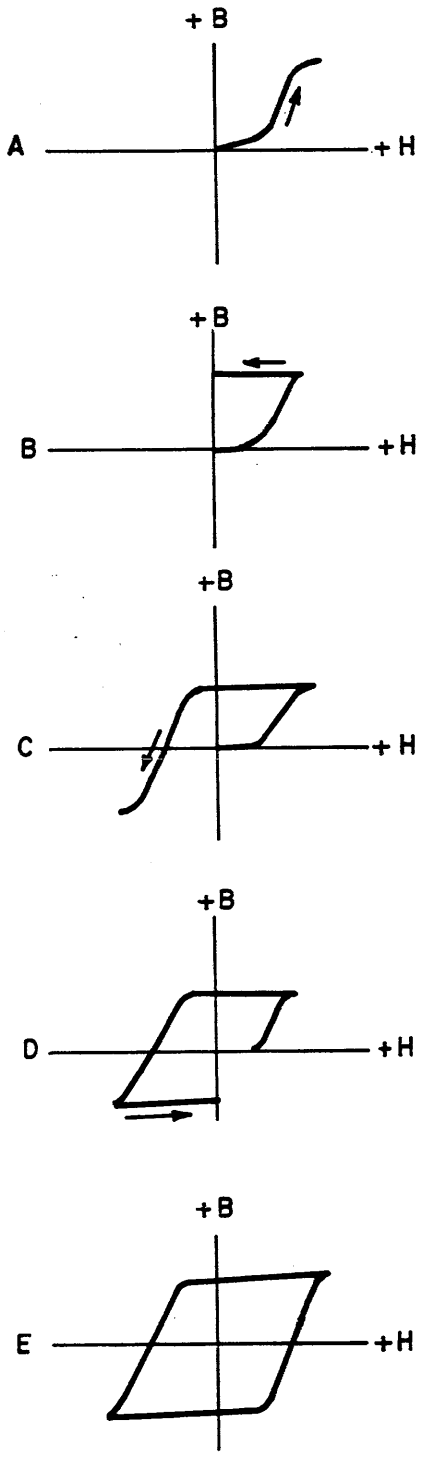
PRINCIPLES OF MAGNETIC CORE MEMORIES

Magnetic Core Storage

The memory core stack, housed in the magnetic core unit, is a matrix configuration of individual (30 mils O.D., 18 mils I.D.) ferrite cores. Basically, the ferrite core is a 1-bit storage element in the form of a ferrite ceramic ring that can be magnetically saturated to either positive of negative flux density. The ferrite material retains a large part of the magnetic flux developed at the time the core is saturated which is an important characteristic of the core. The time required to switch a core from one polarity or state to another is primarily dependent on the core material and size. Consequently, cores measuring only tenths of an inch in diameter are used in the memory core array to permit fast switching speeds.

A similarity exists between the magetic core and the flip-flop in that both provide storage for one bit of data. The two extremes of saturation in a magnetic core represents ZERO and ONE, as do the two stable states of a flip-flop. A core can be set to a ONE state by the application of a current pulse of similar magnitude applied in the opposite direction. Similarly, a flip-flop is set or reset by applying pulses to the appropriate inputs. Both the magnetic core and the flip-flop provide memory of the last pulse applied, but the core does so without requiring power to hold its state.

The ferrite core has a nearly rectangular hysteresis loop. The hysteresis loop is a graphical representation of the flux density produced in a magnetic material, plotted against the magnetizing force that produces it. Figure 2-2-1 is a simplified drawing showing the generation of a typical ferrite core hysteresis loop. Starting with an unmagnetized core, an increase in magnetizing current (H) increases the flux density (B) along the S-shaped curve (A). The flux density levels off when the core is saturated, and any additional current applied does not appreciably increase the flux density because the core material is supporting as much flux as it can. As the current is decreased, then made to flow in the opposite direction, the flux does not collapse along the same line (B); and most of the flux remains even after the current has fallen to zero. The amount of flux actually remaining is a function of the retentivity of the magnetic material. As a magnetizing current is applied in the opposite direction, it has little effect on the flux level until the current reaches the knee of the hysteresis loop.



As Positive Current Increases Rising Flux Density is Limited by Core Saturation

Most of the Flux Remains after the Current is Removed.

As Negative Current Reaches the Switching Point, the Core is Driven to Negative Saturation

As with Positive Current, when Negative Current is Removed, Most of the Flux Remains

Thus, the Core is always Saturated in the Positive or Negative Direction

Figure 2-2-1. Ferrite Core Hysteresis Loop

A slight increase in current beyond the knee of the curve switches the core rapidly to negative saturation (C). The point on the curve representing the amount of current required to change the state of the core is termed the coercive current. When the negative magnetizing current is removed, most of the flux is retained as before (D). Note that the original sweep from a magnetically neutral condition is never repeated (E). A memory core in coincident-current use is never in a neutral condition, but is switched from one saturated state to the other. The core is thus an extremely useful binary component because it can exist in either of two stable states and can switch rapidly from one to the other.

For any given toroidal magnetic core, the necessary magnetomotive force required to effect switching is a function of the product of the number of turns of wire and the current driven through those turns. It is not economically feasible to wind multiple turns of wire around the small toroidal cores used in core memories; rather the number of turns is reduced to two, one in each of the perpendicular driving coordinates, and the current in these coordinate wires is of such a magnitude as to cause switching (rapid flux change) to occur.

In addition to the perpendicular (X and Y) coordinate selection lines, each core is also threaded by two other wires, each of which passes through every core in a plane. One is the sense winding, which detects flux-change due to switching of a core and thus provides a readout signal from the plane. The other winding is the inhibit winding which is used, as its name suggests, to inhibit or prevent the writing of a ONE into the core, thereby causing ZERO to be stored. A single memory core, with its associated control windings is illustrated in Figure 2-2-3.

A disadvantage of the memory core is that it does not provide a static indication of its state, as does a flip-flop. To obtain an indication of the condition of the flux in a memory core, the state of the core must be switched.

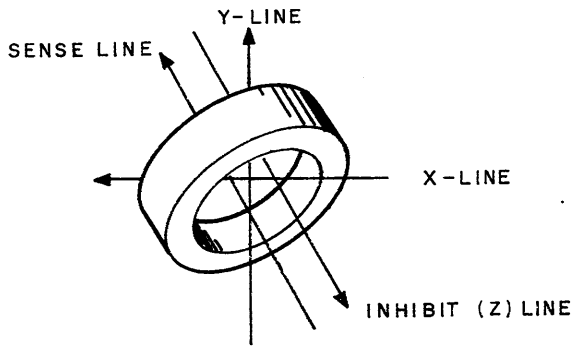


Figure 2-2-2. Core Control Windings

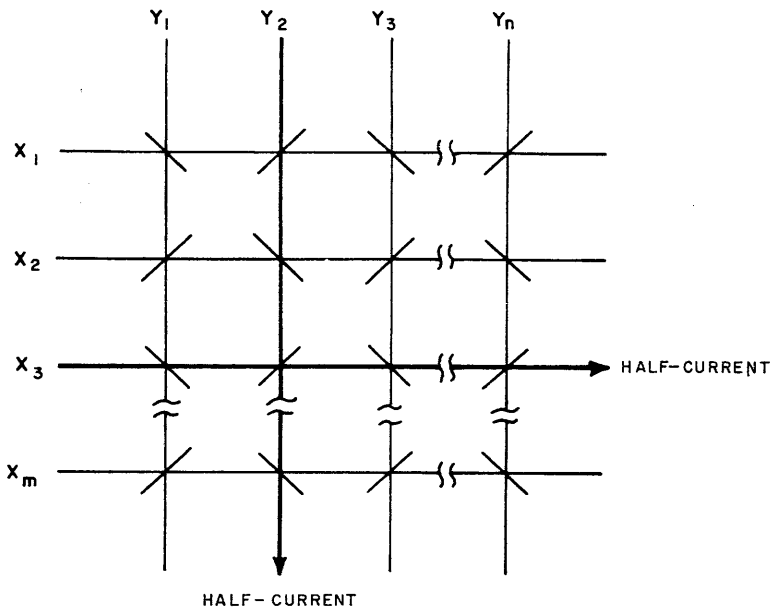


Figure 2-2-3. Coincident-Current Selection

Information Sensing

Sense lines allow the reading of information stored in the cores. One sense line (Figure 2-2-2) is threaded through all memory cores of each mat.

To read any of the words stored in memory, half-currents in the proper direction are generated in the selected X- and Y-lines (Figure 2-2-3). The read half-currents combine at the coincident junction of the X- and Y-lines to change the state of the affected core in each memory mat. If the affected core is storing a ONE at that instant, the effect of the read half-currents will change the state of the core to ZERO. If the core was previously in the ZERO state, the read half-currents will have no effect on the core. When the core is switched from the ONE to the ZERO state, the rapid change in flux from positive saturation to negative saturation induces a voltage pulse in the corresponding sense line. Therefore, the presence of a voltage pulse in the sense line during the read operation indicates that a ONE has been stored in the indicated core. If no voltage pulse occurs in a sense line during read operation, a ZERO is indicated. The sense lines designated SW01 through SW16 in the memory core stack are connected to sense amplifiers. A ONE input to any of the sense amplifiers is amplified and applied to the information register. Thus, output data is transferred from its storage location in the core stack to the information register.

Addressing

The complete core stack for a magnetic core unit consists of a number of individual matrices or mats. Each mat contains memory cores assembled in a rectangular configuration. The memory cores are threaded by X- and Y-lines in each mat so that one memory core is physically located at each junction of an X-line and Y-line.

As previously stated, pulses of current applied along the X- and Y-lines switch a memory core from one state to another. If one-half of the current required to switch a core is applied along the X-line, and one-half of the necessary current is applied along the Y-line, the core situated at the junction of the energized X- and Y-lines will receive the full switching current. This type of operation is termed coincident-current operation.

A coincident-current magnetic core memory depends upon the coincidence of two half-currents to read data from or to write data into the cores. Two additive half-current pulses will set the core to the ONE state, while two half-current pulses applied in the opposite direction will reset the core to the ZERO state. A core with two half-current inputs is essentially an AND circuit requiring that half-current be applied to both X- and Y-lines in the same direction to change the state of the flux at the core. A half-current applied to one line without a similar half-current applied to the other line has no effect on the core.

Only one X-line and one Y-line of a mat are energized during a single cycle, and only that core situated at the junction of the activated X- and Y-lines will respond to the coincident half-current pulses. Therefore, only one core in each mat will be affected during a single cycle. A simplified diagram of coincident-current selection of a memory core is illustrated in Figure 2-2-3. In effect, the X-line selects one row (X-row), and the Y-line selects one column (Y-column).

In coincident-current memories, the X- and Y-lines are wired in series through all mats of the memory core array. Thus each X-line and each Y-line threads corresponding rows or columns of cores in all memory mats. Energizing one of the X-lines (designated X_1 through X_m in Figure 2-2-3 supplies a half-current pulse to the appropriate row of cores in every mat. Similarly, energizing one of the Y-lines (designated Y_1 through Y_n), supplies a half-current pulse to the appropriate column of cores in every plane. When pulses occur simultaneously on two lines (X and Y), they select the same core position in each of the planes. Therefore, the X- and Y-lines select a word in the memory core array and enable read or write operations.

Writing

Inhibit lines are used to enable a computer word or instruction to be written into memory at a selected address location. A single inhibit line is threaded through each memory core in a mat (Figure 2-2-4) and each mat of the magnetic core stack requires an individual inhibit line.

To write information into memory, half-current pulses in the direction opposite to those generated for read operation are applied to the selected X- and Y-coincident junction to switch the affected core in each memory plane.

Since all the cores at the selected address have been cleared to the ZERO state prior to the application of the write half-currents, the write half-currents operate to switch all cores to the ONE state. If the incoming data dictates that a ZERO is to be written into a specific core, some means must be used to prevent the core from switching to the ONE state when the write half-currents are generated. This is accomplished by the inhibit (Z) lines designated ZW01 through ZW16. An inhibit pulse, when transmitted through the inhibit line of the memory plane at the same time that the write half-currents are applied through the X- and Y-lines, prevents the writing of a ONE because the inhibit current subtracts from X- and Y-write current.

The inhibit pulse is of the same magnitude but of the opposite polarity to the write half-current pulses. Therefore, the inhibit pulse directly cancels the effect of one write half-current pulse. The net effect of the two write half-current pulses and an inhibit pulse, is equivalent to a single write half-current pulse on the addressed core. This prevents the core from switching from the ZERO to the ONE state.

Information to be written into memory is stored in the information register prior to being transferred to the memory core stack. During the transfer operation, a passive signal from the register flip-flop will prevent the generation of an inhibit pulse whereas an active signal from the register flip-flop allows an inhibit pulse to be generated. In this way information is rewritten (or new information is written) into the selected memory location exactly as it appears in the information register.

CORE STACK CONFIGURATION

The storage array is organized about a conventional four-wire "3D" configuration where 4096 addressed cores are made available by the intersection of 64 X lines and 64 Y lines in each bit area.

ADDRESSING AND SELECTION

Addressing-Random Access

The memory address register consists of cross-coupled flip-flops located on the CM-306 Selector PAC. Data received by the 12 single-ended, address input lines (MAD05 through MAD16) will set the flip-flops and a reset pulse (MADCL-) will commonly reset all the flip-flops at the end of the cycle. The address flip-flop outputs control the drive line selection circuits. Section 5 contains a detailed description of this PAC.

Decoding and Selection

Figure 2-2-4 is a simplified diagram of the address decoding and selection for a typical bit of a 4K memory. Three address bits are transferred to the X switches and three others to the X sinks. The X switches uniquely enable one of eight read/write line pairs going to the diode matrix; the X sinks select one of eight read/write busses. The selected buss enables one end of eight drive lines, each of which has its other end connected to an enabled diode matrix. Thus, only one of 64 X lines has been selected. The Y-line selection is accomplished in a similar manner.

Figure 2-2-5 is a simplified schematic diagram of the X decoding and selection matrix. Two diodes per line isolate a single line when selected. Consider a read-regenerate cycle involving drive line X60. During the read portion of the cycle, X read switch (Q1) and X read sink (Q4) are selected by related address register outputs. These selection outputs are turned on when read timing pulses XRSW- for the switch and XYRE- for the sink go to 0V. Read current then flows in line X60 from +15V through R1, Q1, CR1, CR2, X60, and Q4 to ground. Read current ceases to flow when signals XRSW- and XYRE- return to +6V. During the write portion of the cycle the addresses do not change. Write timing pulses XYWE- for the sinks and XWSW- for the switches are generated. When these signals go to 0V, sink Q2 and switch Q3 are turned on. Write current then flows from +15V through R1, Q3, CR3, line X60, CR4 and Q2 to ground. Write current ceases when signals XYWE- and XWSW- return to +6V. At the end of the cycle, the addresses will change and, by similar manner, the remainder of the X lines will be selected.

The Y-selection matrix is similar to the one described with the exception of being decoded by different addresses and command signals. For a detailed description of the CM-306 Selector PAC, refer to Section 5.

TIMING AND CONTROL

Section 4 contains the timing and control logic diagrams to illustrate the logical functions associated with the control and distribution of memory timing pulses. Interface timing is presented in Figure 2-1-2.

OPERATING MODES

Read-Regenerate Mode

Memory interface signals are provided by the CPU or the memory expansion option. When the Selector PAC control pulses XRSW- and XYRE- are generated, the sinks and switches are turn on. Stored data present in the address register will be read out (Figure 2-2-6). The sense amplifier strobe input (STROB-) will sample the data. If a ONE was stored at that address, the sense amplifier associated with that bit will produce an output, setting the data registers external to the memory module. The set side of the data registers (MXXFF+) will be presented to the input of the inhibit drivers and disable it. If a ZERO was stored at that address, no output will occur. The data register will remain reset and enable the inhibit drivers. During the write portion of the cycle, the selector PAC

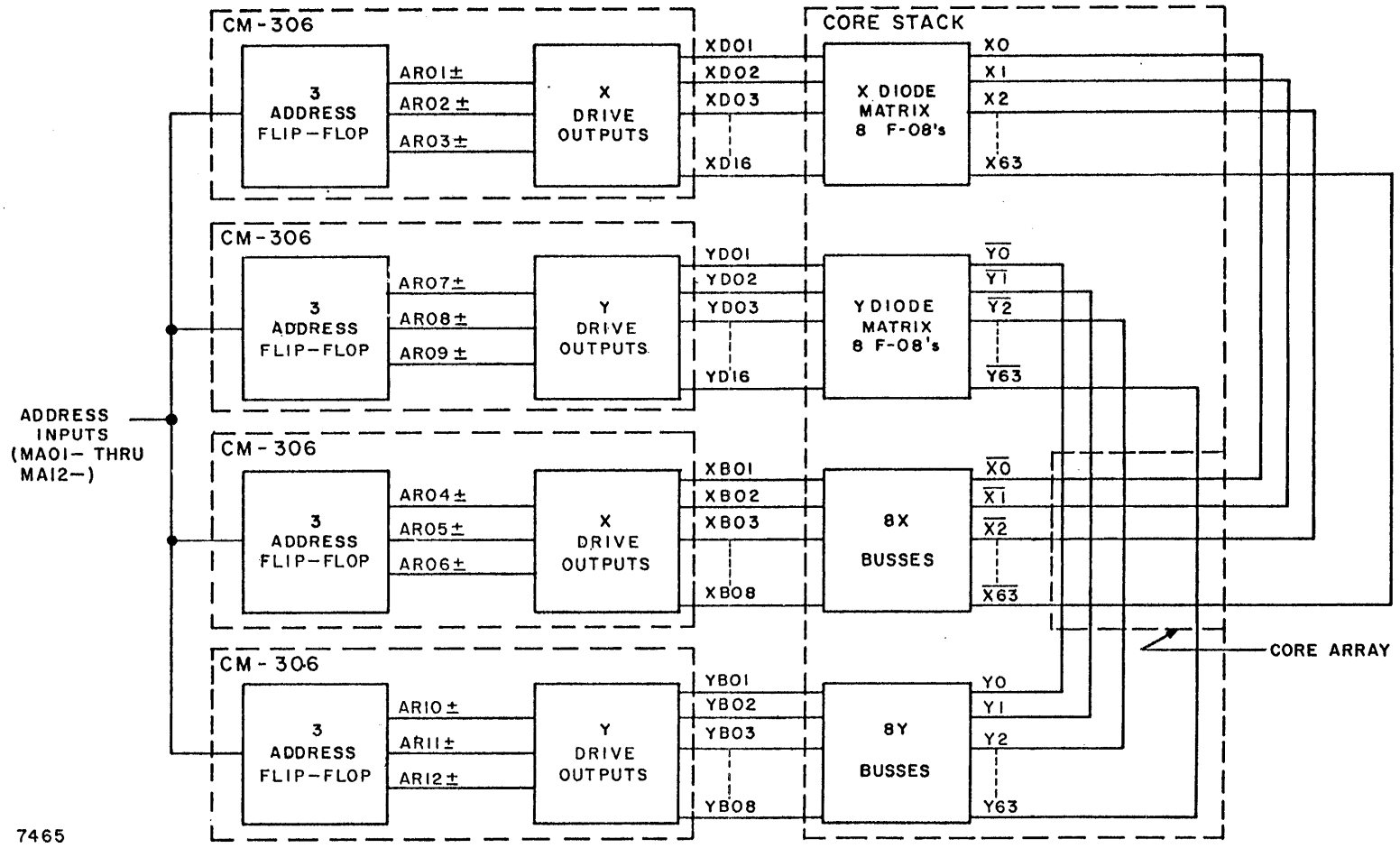


Figure 2-2-4. Address Decoding and Selection, Simplified Block Diagram

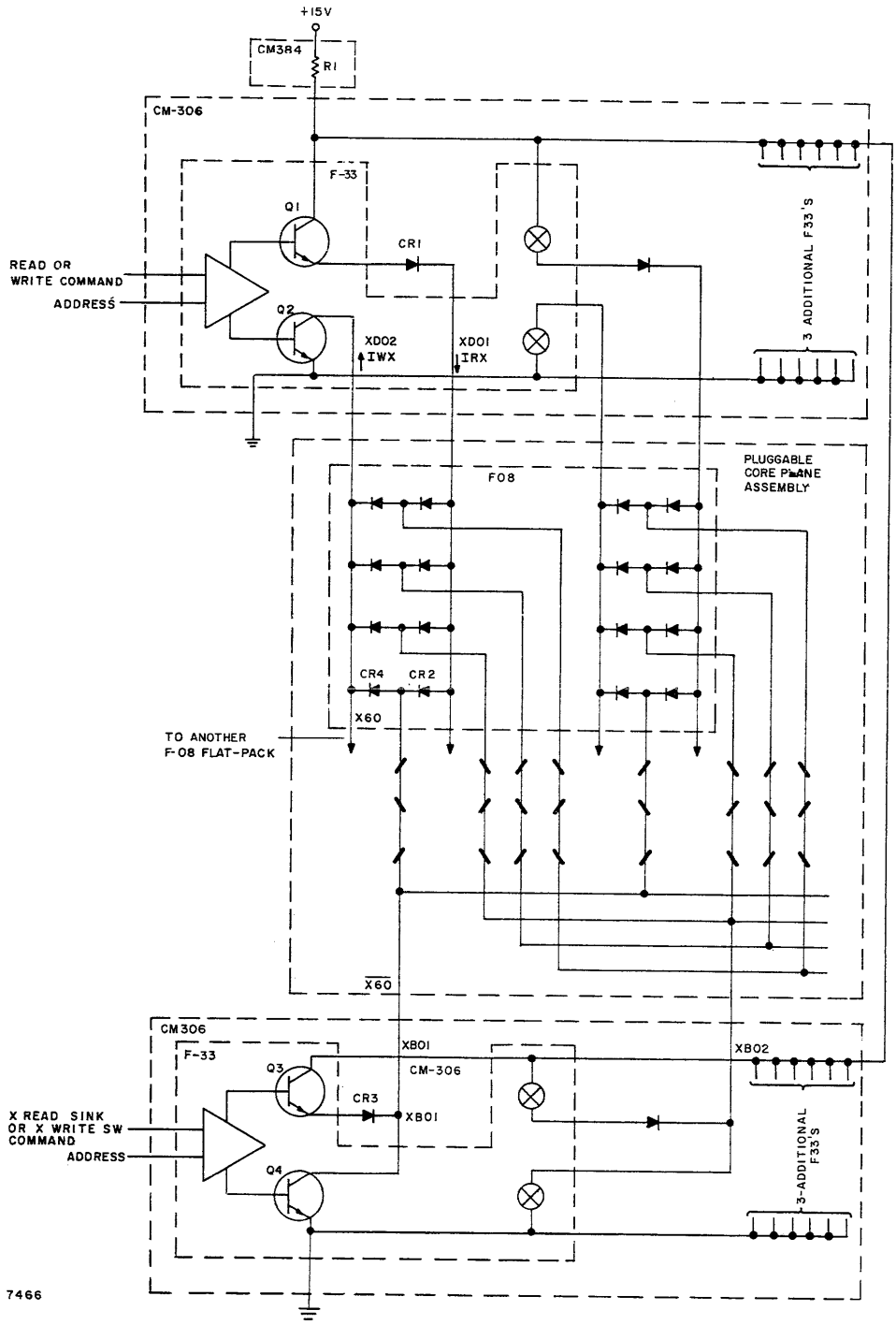


Figure 2-2-5. Decoding and Selection Matrix, Simplified Schematic

control pulses (XRSW- and XYWE-) are generated, and X- and Y-line currents are once again established. When the inhibit pulse (INHBX+) is generated, a ONE will be inserted into the stack if the inhibit drivers were disabled. A ZERO will be reinserted if the drivers were enabled.

Clear-Write Mode

The clear-write mode operation is identical to the read-regenerate mode except the sense amplifier strobe signal is not generated. Without the sense amplifier strobe, data stored in a selected address are destroyed. During the write portion of the cycle, new information stored in the data register is inserted in the core stack in the same manner that information is regenerated.

INTERFACE TIMING

The interface timing for the read-regenerate and clear-write modes is shown in Figure 2-1-2. The timing distributor does not form an integral part of the memory system, therefore, with the exception of signals XYRE-, XYWE-, XRSW-, and XWSW-, all signals, whether used internally or as commands, are classified as interface timing.

The address inputs (MAD05 through MAD16-) must be present for all cycles for the duration shown on the interface timing diagram. The data lines (M01FF+ through M16FF+) must be stable for the duration of the INHBX+ pulse as defined on the timing diagram for a read-regenerate or clear-write cycle.

MEMORY RETENTION

The magnetic core array does not require power to provide a static memory capability. A pulse of power is required to switch cores from one state to the other, but the pulse is not necessary to hold cores in their respective states. All cores remain in the state to which they have been switched because of material retentivity in the core. If power is removed or lost, the magnetic core array retains stored information indefinitely.

The turn-on sequencing of the main power supply is designed to allow the +15 voltage to remain off until the +6V and -6V logic supplies are stabilized. Similarly, the +15V supply is turned off before the logic supplies go out of regulation. This feature ensures that no current can flow during the power supply turn-on and turn-off transients providing memory input commands are quiescent which might change data previously stored in the core array.

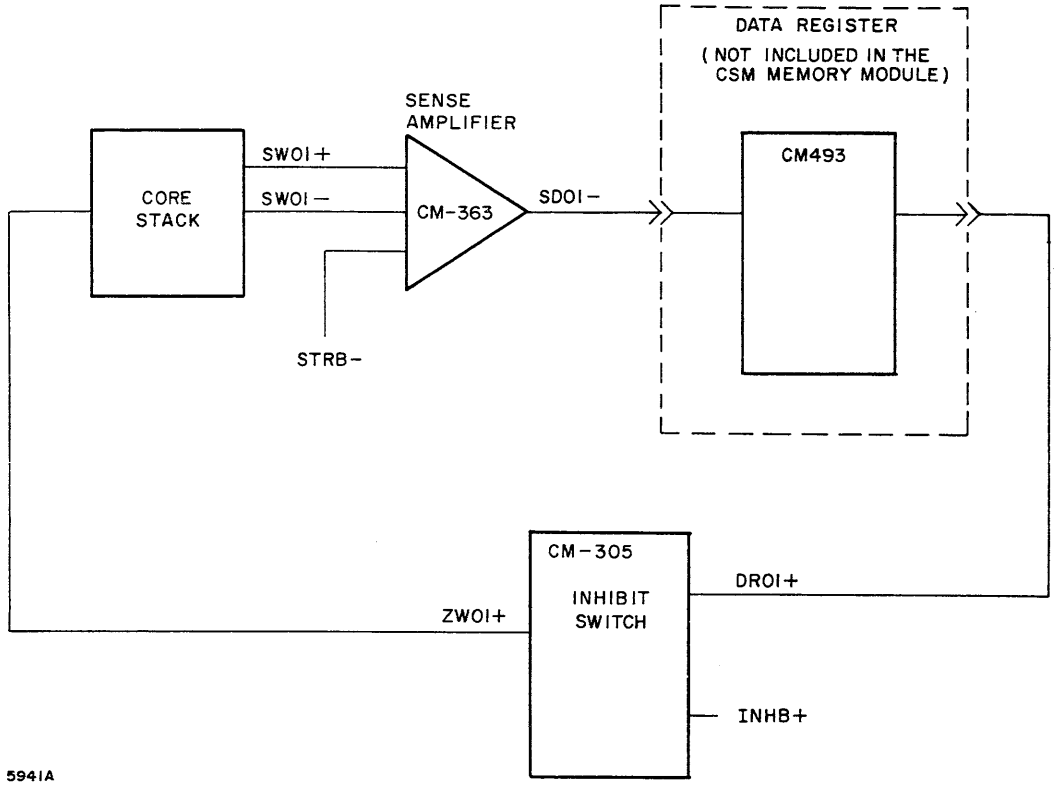


Figure 2-2-6. Regeneration Loop, Simplified Diagram

INTERFERENCE FROM MAGNETIC FIELD

Fan motors or power supplies having large magnetic fields should not be mounted close to the core stacks (some fan motors have fields that exceed 10 gauss). Reliable memory operation is guaranteed only if the peak magnetic field is held below 3 gauss in the region of the core mats.

SECTION 3
MAINTENANCE

This section contains data on preventive and corrective maintenance, service and repair for the H316 Magnetic Core Memory Module. Detailed PAC descriptions are included in Section 5 of this chapter.

TOOLS AND TEST EQUIPMENT

Table 2-3-1 lists the tools and test equipment required to service the memory. Detailed information on wire-wrapping tools and procedures is contained in the Instruction Manual for Solderless Wrapping of μ-PAC Digital Modules, Doc. No. 70130071371.

RECOMMENDED SPARE PARTS

One spare PAC of each type specified in Section 4 (LBD 80.08) is recommended as a spare part. Two F-08 microcircuits (70950100008) are recommended as spare parts if a spare corestack is not purchased. Section 5 contains parts lists for all PACs in the memory.

PAC HANDLING AND REPAIR PROCEDURES

Inserting and Removing System PACs

The μ-PAC connector is polarized to protect against incorrect PAC insertion. μ-PAC removal from the memory is accomplished by engaging the two holes in the handle of the PAC with the μ-PAC extractor tool. Do not remove or insert printed circuit cards without turning off the dc power to the unit.

PAC Troubleshooting

The Extender PAC, Model XP-330, can be used to gain access to points on the μ-PACs. Signals on the pins of the μ-PACs may be ascertained from the PAC descriptions contained in Section 5.

Component Checking

Many μ-PACs have identical channels. Components can be checked by resistance comparison with parts on other channels or other μ-PACs.

Component Replacement

When replacing defective components, use a low-wattage soldering iron and rosin core 60/40 solder. Remove excess solder from the printed circuit board. Care should be taken to avoid lifting the etch.

Table 2-3-1
Tools and Test Equipment

Quantity	Description	Type (or Equivalent)
1	Oscilloscope	Tektronix 585
1	Dual-Trace Preamplifier	Tektronix 82
1	Multimeter	Simpson 260
1	Card Extender PAC	XP-330
1	μ-PAC Extractor Tool	B008428
1	AC Current Probe	Tektronix P6016 probe and passive termination (or type 131 amplifier)
1	Hand Wire-Unwrapping Tool	70 917 202 001 (Gardner-Denver 505084-LH)
1	Hand Wire-Wrapping Tool, Battery Operated	70 917 200 001 (Gardner-Denver No. 14R2)
1	Wire Stripper	70 917 250 001 (Ideal 45-179)
25 ft	No. 30 AWG Solid Wire	70 940 061 010
1	Quick Disconnect Terminal Crimper	T and B WT 145
25 ft	No. 30 AWG Twisted-Pair Solid Wire	70 940 402 002
1	Precision DC Voltmeter	Weston Model 931-1905003 30/7 5/3 volts, ±1/2%, 1000 ohms/volt

Insert the leads of the new component through the drilled hole or eyelet, clip off excess wire, and solder to the printed circuit etch. A flat pack should be placed squarely on the etched area, using an insulator between it and the μ-PAC (except F-33 use Insulgrease instead of insulator). The leads should then be cut to the proper length and soldered. Examine the PAC carefully for excess solder. Remove rosin deposits with a commerical cleaning solvent and wipe the PAC clean with a dry lint-free cloth.

MAINTENANCE INSPECTION

Conduct a visual inspection periodically. Watch for accumulation of dust, dirt, improperly seated PACs, and damaged or improperly dressed cable and signal leads. Check to see that all connectors are securely mated and that the cooling fans are operating properly. Clean fan filters periodically. Do not clean core stack with air hose.

PREVENTIVE MAINTENANCE PROCEDURE

The memory is thoroughly tested at Honeywell Inc., Framingham, Mass., prior to shipment. All planes are tested simultaneously under all ZEROs, all ONEs, and worst-pattern conditions. The drive currents and strobe timing are set so that optimum operating margins result. The memory should be tested periodically, as a preventive maintenance procedure, by using a memory test program.

Memory Drive and Inhibit Voltage Calibration

The memory drive and inhibit currents are determined by the setting of the +15 Vdc supply and the CM-384A precision resistors. The +15V supply setting should be periodically checked by using a voltmeter capable of reading the voltage within ±1%. Measurements should be made at the memory terminals while a program is running in the memory.

The +15 Vdc supply should be within the following ranges as a function of stack inlet ambient temperature.

Temperature	+15 Vdc Range
0°C	+16.0 ± 0.6V
25°C	+15.0 ± 0.8V
50°C	+13.8 ± 0.6V

The memory may be operated at marginal +15 Vdc supply for corrective or preventative maintenance purposes. The diagnostic program should contain at least the worst pattern (exclusive-OR of MA01-, MA03-, MA04-, MA07-, MA09-, and MA10-), all ONEs and all ZEROs. Failure points at high +15V setting (do not exceed +17.5V) and low +15V setting should be noted; their differences should be at least 1.6V at 0°C and 25°C and 1.1V at 50°C. The +15V supply may be set at the center of the failure point margins or at the values shown above.

Strobe Timing Calibration

The timing of the sense amplifier strobe pulse is set for each unit to give optimum operating margins. It should not be necessary to adjust the strobe timing. If a change in timing is required to obtain proper memory operation, the associated PACs should be checked (e.g., CM-306, CM-305) before a timing change is made. The CC-373 description in the Appendix should be referred to if a timing change is required. The STROB- pulse should be between 150 ns and 200 ns wide at the 1.5V points.

CORRECTIVE MAINTENANCE PROCEDURES

Memory system troubleshooting consists of determining the type of problem, predicting the μ-PAC at fault, and locating the faulty circuit. Test procedures to aid in troubleshooting are as follows.

CAUTION

Use oscilloscope probes carefully to avoid shorting of connector terminals resulting in damage to the PAC.

a. In some cases, spare PACs may be used to isolate faulty circuits by interchanging identical PACs and noting any shift in the faulty bits or addresses. All memory PACs with the same designation are interchangeable.

b. Refer to PAC schematic and assembly drawings in Section 5 to isolate the defective components on the printed circuit card. Replace defective components.

c. Memory failures are generally of the following types:

(1) Operation failures, which are caused by faulty timing and control circuits.

(2) Partial data word failures caused by a faulty sense amplifier, data register flip-flop, or data regeneration circuits.

(3) Address failures caused by faulty address register or selection circuits.

d. Memory failures may be localized by the following procedures:

(1) Load the test pattern into the memory.

(2) Initiate a read operation at each address sequentially and check each readout data word for the following failures:

(a) Operation failures: No apparent response to commands applied to the memory, or faulty operation at all addresses (Table 2-3-3).

(b) Partial data word failures: Failures of one bit or series of two or more bits at all addresses (Table 2-3-4).

(c) Address failures: Faulty memory operation at particular addresses only (Table 2-3-5).

MAGNETIC CORE STACK MAINTENANCE

Under normal operating conditions, it is unlikely that troubles will occur within the magnetic core stack. However, continuity measurements of the sense inhibit and drive windings will enable maintenance personnel to check core stack wiring. Exercise caution in taking these measurements to avoid damaging the matrix windings.

CAUTION

Multimeter current and voltage should be kept below 300 mA and 30V, respectively, to avoid damage to matrix windings and components.

Sense Windings

a. Turn off memory power. Remove the Sense Amplifier PAC, CM-363A associated with the sense windings to be checked.

b. Place the ohmmeter leads across the sense winding inputs (SWXX+ and SWXX-) to the Sense Amplifier PAC as determined from the logic diagrams of Section 4 and check for continuity. One sense winding links 4096 cores (Table 2-3-5).

Table 2-3-2
Operational Failures

Symptoms	Probable Fault
No apparent response to commands	1. DC voltage 2. CC-373 PAC 3. MBSYX-, MEMCI+, RTDL- signals
Unable to read from any address	1. CC-373 PAC 2. 15.5 volt supply 3. STROB- Signal

Table 2-3-3
Partial Word Failures

Symptoms	Probable Fault
Failure of one bit (ZERO or ONE) at all addresses	1. Sense Amplifier PAC (CM-363A) 2. Data register 3. Inhibit PAC 4. Sense winding 5. Inhibit winding 6. Resistor PAC
Failure of one bit at particular addresses	1. Sense Amplifier PAC 2. X or Y-switch or sink PAC 3. Sense winding 4. X or Y-drive line 5. X or Y-selection diode (F-08)
Failure of one bit at one address	1. Marginal Sense Amplifier PAC 2. Marginal core

Table 2-3-4
Address, Decoding, and Selection Failures

Symptom	Probable Fault
All bits fail as a function of particular address bits	1. X or Y-switch or sink PAC 2. CC-363A PAC 3. X- or Y-drive line 4. X- or Y-selection diode

c. Resistance readings should be approximately 28 ohms for all sense windings. The resistance readings for all bits should agree within ±10%.

Drive Windings

a. Turn off memory power. Remove the Selector PAC, CM-306 associated with the X- and Y-drive line to be checked. This can be determined from the logic diagrams by relating the bad address to a sink and switch output for both the X- and Y-coordinates. The drive winding connections to the core stack are shown in Figure 2-1-1.

b. The actual drive line connections are located on the core stack printed circuit board. The selection switch outputs are isolated by a diode from each drive line so that the resistance reading between any dual bus (XDXX) and line bus (XBXX) will include a diode forward drop.

c. Measure continuity by referring to the simplified selection diagram, Figure 2-2-5. For example, to check the continuity of drive line X60, put one ohmmeter probe on the corresponding sink output (collector output of transistor Q4) and the other ohmmeter probe on the proper switch output (collector of transistor Q2). A low resistance (one forward diode drop plus a drive line resistance of approximately 6 ohms) indicates continuity for both diodes and the drive line. It may be necessary to reverse the probes to obtain the correct polarity to forward-bias the selection diodes. The continuity of the current path for the opposite drive polarity should be similarly checked by moving the probe from the collector of Q2 to the emitter of Q1 and reversing the polarity. In this mode of measuring, two diodes will be in the circuit. A high resistance reading in both drive current polarity paths indicates an open drive winding or drive bus. If a drive bus is open, the other drive lines connected to the same bus will also have a high resistance reading. A high resistance reading in only one of the read or write current paths indicates an open F-08 flat pack diode.

Inhibit Windings

a. Turn off memory power. Remove the Inhibit PAC CM-305 associated with the inhibit line to be checked.

b. Place the ohmmeter leads across the inhibit winding inputs (ZWXX+ and ZWXX-) to the Inhibit PAC as determined from the logic diagram of Section V and Table 2-3-6.

c. Resistance readings should be approximately 11 ohms for all inhibit windings. The resistance windings for all bits should agree within ±10%.

Table 2-3-5
Sense Winding Check List

Sense Winding	Location	Sense Winding	Location
SW01+	A1BX0323	SW09+	A1BX0114
SW01-	A1BX0321	SW09-	A1BX0116
SW02+	A1BX0319	SW10+	A1BX0110
SW02-	A1BX0317	SW10-	A1BX0112
SW03+	A1BX0315	SW11+	A1BX0124
SW03-	A1BX0313	SW11-	A1BX0122
SW04+	A1BX0311	SW12+	A1BX0118
SW04-	A1BX0309	SW12-	A1BX0120
SW05+	A1BX0324	SW13+	A1BX0123
SW05-	A1BX0322	SW13-	A1BX0121
SW06+	A1BX0318	SW14+	A1BX0119
SW06-	A1BX0320	SW14-	A1BX0117
SW07+	A1BX0314	SW15+	A1BX0115
SW07-	A1BX0316	SW15-	A1BX0113
SW08+	A1BX0310	SW16+	A1BX0111
SW08-	A1BX0312	SW16-	A1BX0109

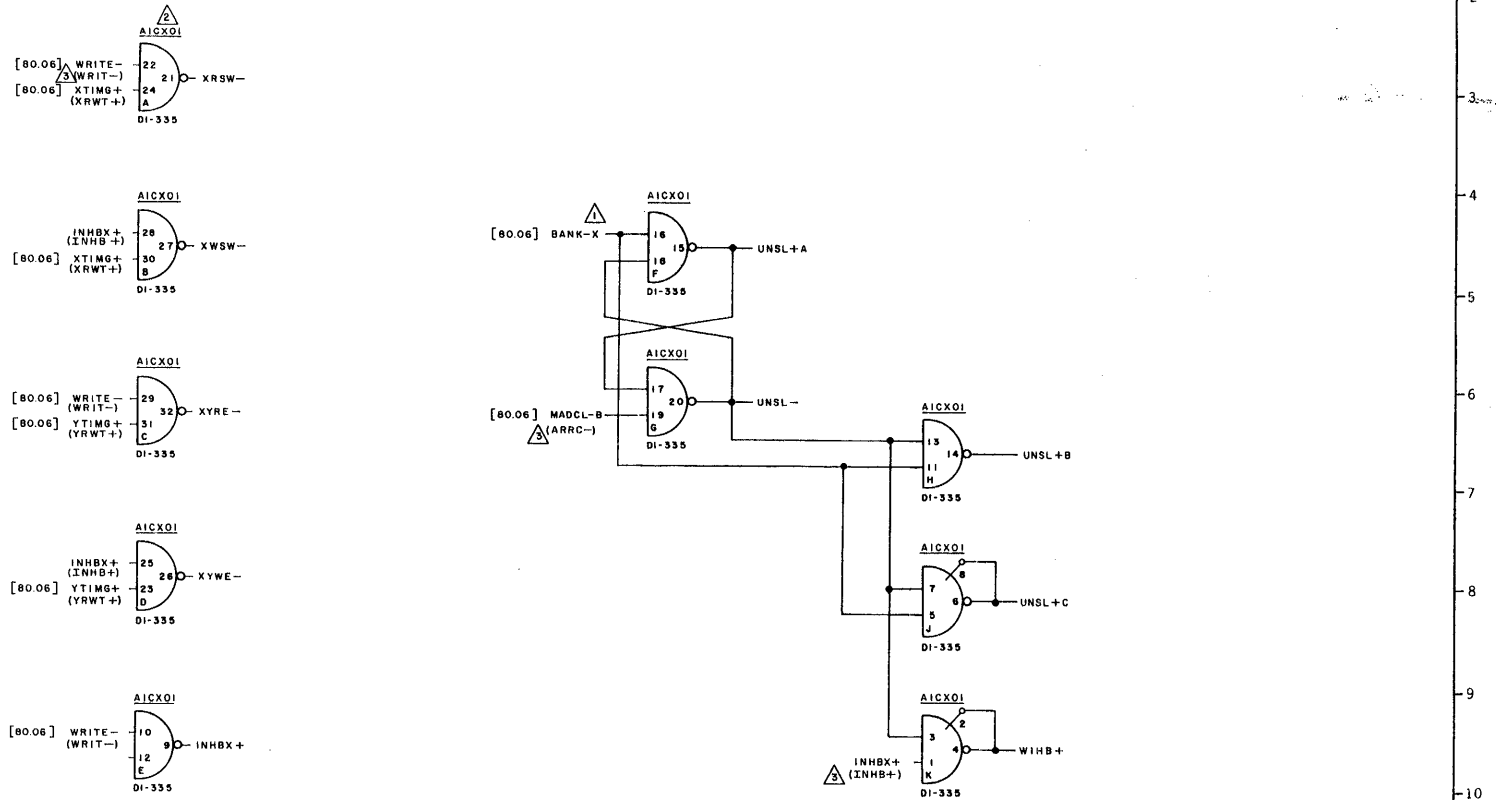
Table 2-3-6
Inhibit Winding Check List

Sense Winding	Location	Sense Winding	Location
ZW01+	A1CX0603	ZW09+	A1CX0406
ZW01-	A1CX0601	ZW09-	A1CX0408
ZW02+	A1BX0632	ZW10+	A1AX0426
ZW02-	A1BX0631	ZW10-	A1AX0428
ZW03+	A1BX0601	ZW11+	A1CX0607
ZW03-	A1BX0602	ZW11-	A1CX0605
ZW04+	A1AX0631	ZW12+	A1AX0627
ZW04-	A1AX0629	ZW12-	A1AX0625
ZW05+	A1CX0402	ZW13+	A1BX04-30
ZW05-	A1CX0404	ZW13-	A1BX04-29
ZW06+	A1BX0432	ZW14+	A1BX04-03
ZW06-	A1BX0431	ZW14-	A1BX04-04
ZW07+	A1BX0401	ZW15+	A1BX06-30
ZW07-	A1BX0402	ZW15-	A1BX06-29
ZW08+	A1AX0430	ZW16+	A1BX06-03
ZW08-	A1AX0432	ZW16-	A1BX06-04

SECTION 4
LOGIC BLOCK DIAGRAMS

This section contains the following logic block diagrams. The logic block diagram (LBD) number is shown in the upper righthand corner of each drawing.

LBD No.	Dwg. No.	Description
80.00	C70022843	Timing and Control
80.01	C70022835	X-Selection Sinks and Switches
80.02	C70022836	Y-Selection Sinks and Switches
80.03	C70022837	X- and Y-Selection Diode Matrix
80.04	C70022838	Sense Amplifiers
80.05	C70022839	Inhibit Drivers
80.06	C70022840	1 x 3 Connector Wiring
80.08	C70022841	PAC Complement and Allocation
---	P70022841	Parts List



NOTES:

1. "X" DESIGNATES A, B, C & D FOR H-316 MODULE A, B, C & D RESPECTIVELY OR 1, 2, 3 & 4 FOR CSM-160 MODULE 1, 2, 3 & 4 RESPECTIVELY. SEE LBD 80.06 TABLE I AND NOTE 1.
2. "X" DESIGNATES MODULE LOCATION G, H, I & J FOR H-316 MODULE A, B, C & D RESPECTIVELY.
3. CSM-160 NOMENCLATURE IN PARENTHESIS.

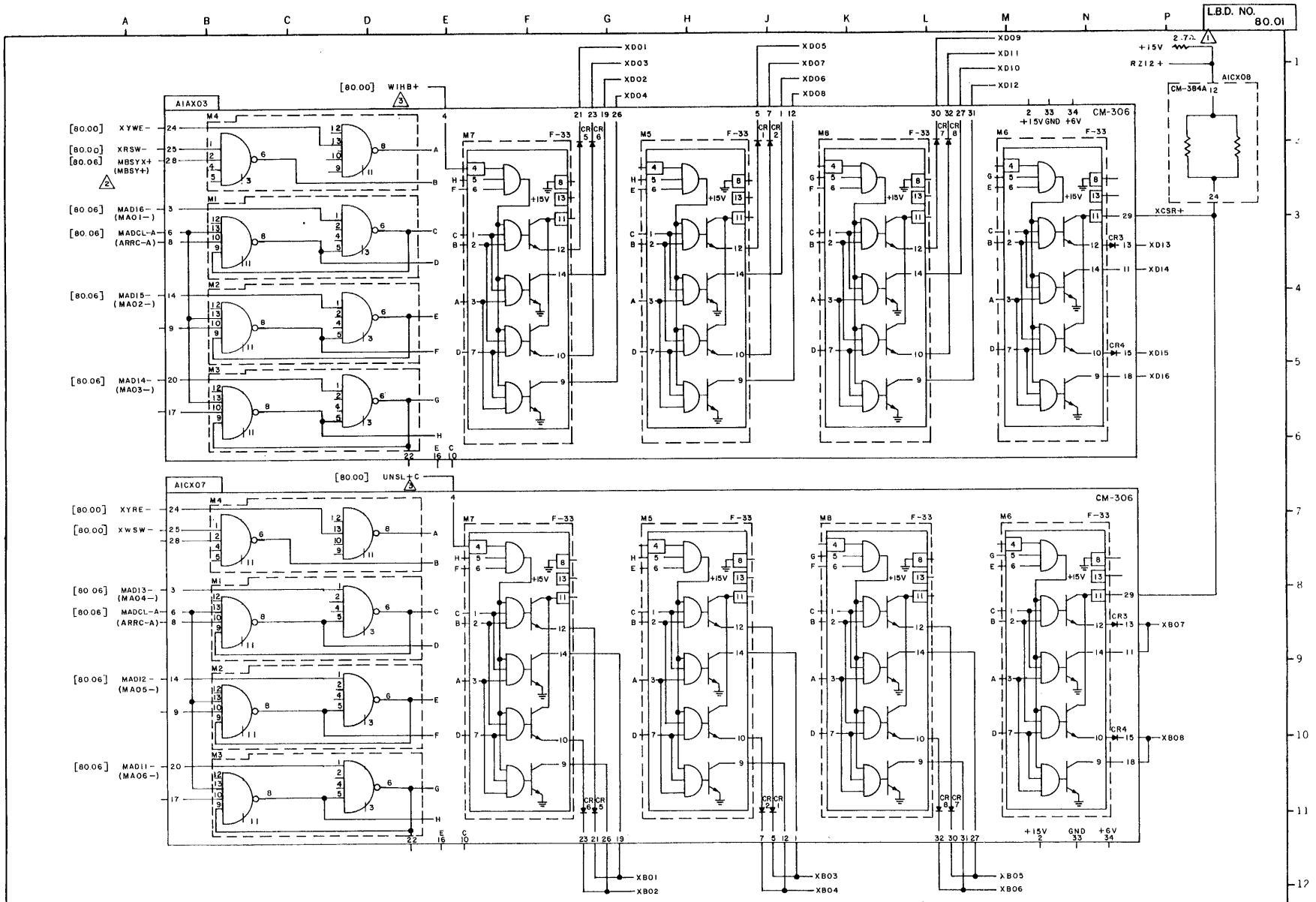
REV.	REVISIONS	CHK.
A	TAKEN FROM S.R. SY 33.3	
B	ECO R-6872 EXT CHANGES P B SEE ECO 5/27/69	
C	ECO 7402 EXT CHANGES SEE ECO 10/13/69	
D	ECO 9423 EXT. CHGS SEE ECO 6/22/71 A.K.	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR.	D. HAMEL	DATE 1/24/69
ENG.	D. DAVIES	1-29-1969
APP.	C. Haas	2-12-1969
PROJECT NO.	55202	

TITLE: CSM-160 AND H-316 MEMORY TIMING CONTROL

SIZE C | DWG NO. 70022843 | REV. D



NOTES:

1. 8 BIT MEMORIES ONLY.
2. CSM-160 AND ICM-160 NOMENCLATURE IN PARENTHESIS.
3. ICM-160 HAS PIN 4 OF ALL CM-306 PACS CONNECTED THRU A 1KΩ RESISTOR TO +6 VDC.

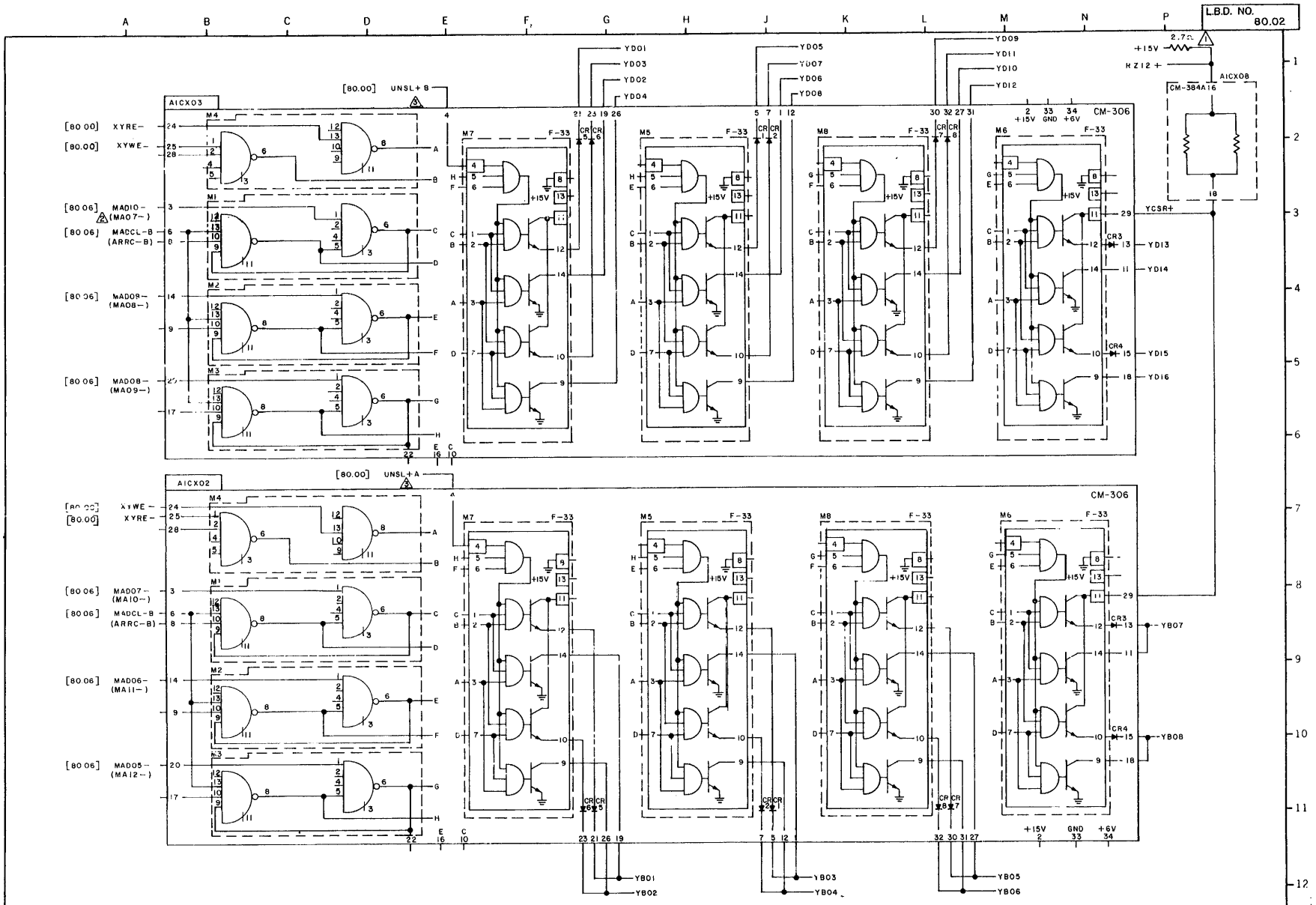
CHK	REVISIONS	REV.
	TAKEN FROM TR. 54-333	A
	ECO R-6872	B
	TEXT CHANGES P.B SEE ECO 5/27/69	C
	ECO 7402 EXT CHAGNES P.B SEE ECO 10/13/69	D
	ECO 8356 EXT. CHGS SEE ECO 5/18/70 A.K.	E
	ECO 8360 EXT. CHGS SEE ECO 6/20/70 A.K.	F
	ECO 9423 EXT. CHGS SEE ECO 6/23/71 A.K.	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR.	D. HAMEL	DATE 1/27/69
ENG.	D. DAVIES	1-27-1969
APP.	C. Haase	2-12-1969
PROJECT NO.	55202	

TITLE
CSM-160, ICM-160 AND H-316 MEMORY X SELECTION SINKS & SWITCHES

SIZE	DWG NO.	REV.
C	70022835	F



NOTES:

1. 8 BIT MEMORIES ONLY.
2. CSM-160 AND ICM-160 NOMENCLATURE IN PARENTHESIS.
3. 1K OHM RESISTOR TO +6 VDC FOR ICM-160.

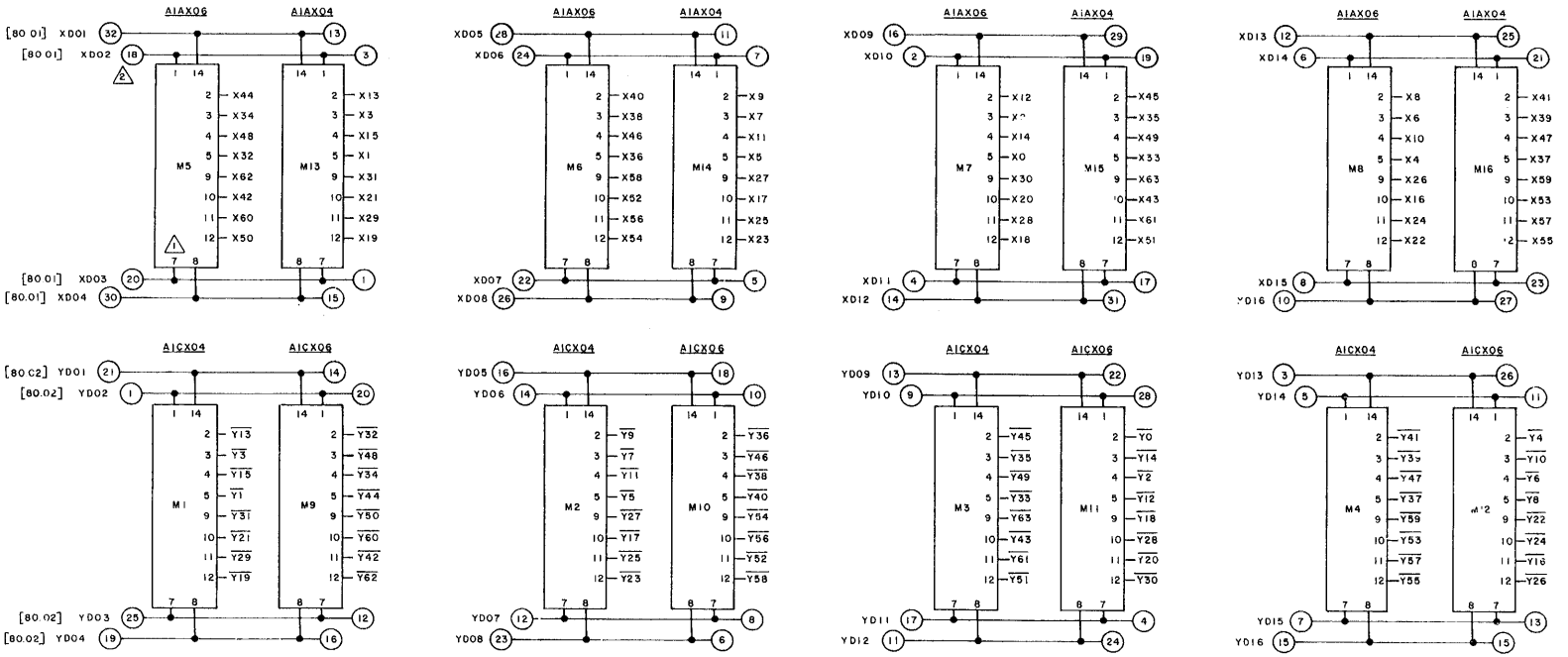
REV.	REVISIONS	CHK.
A	TAKEN FROM S.R. #54.3313	
B	ECO R-6872 EXT CHANGES P 8 SEE ECO 5/27/69	
C	ECO 7402 EXT CHANGES SEE ECO 10/13/67	
D	ECO 8356 EXT. CHGS SEE ECO A.K. 5/18/70	
E	ECO 8360 EXT. CHGS SEE ECO A.K. 5/20/70	
F	ECO 9423 EXT CHGS SEE ECO A.K. 6/23/71	

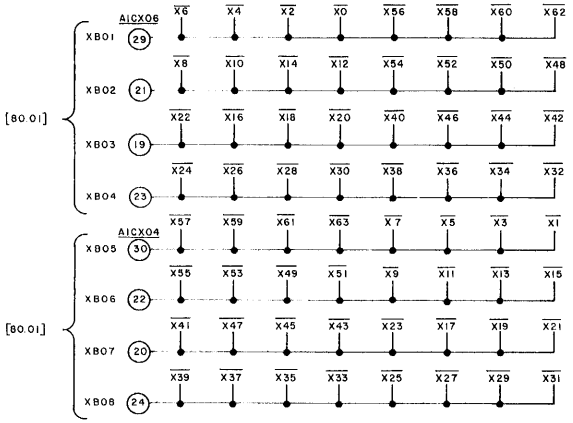
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham Mass

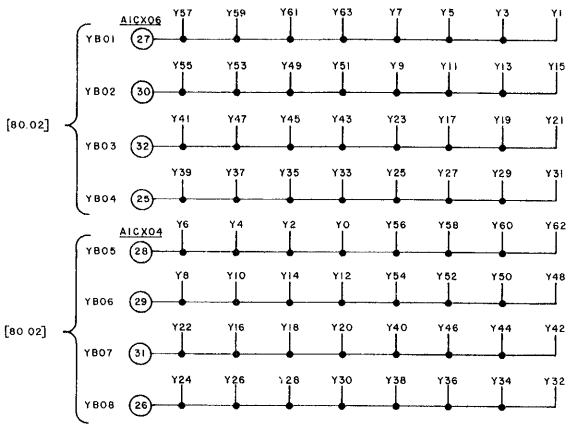
DR.	D. HAMEL	DATE 1-27-69
ENG.	D. DAVIES	1-27-1969
APP.		2-12-1969
PROJECT NO.	55202	

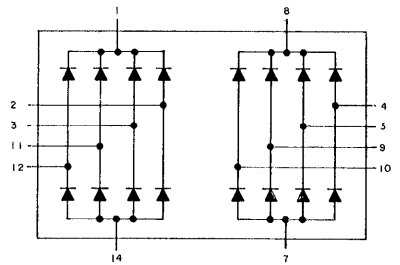
TITLE
CSM-160, ICM-160 AND H-316 MEMORY Y SELECTION SINKS & SWITCHES

SIZE	DWG NO.	REV.
C	7002283	F









TYPICAL F-08 FLAT PAC CONNECTIONS
(M1 THRU M16)

NOTES:

1. 7 — PIN No. OF FLAT PAC (F-08)
2. (18) PIN No. OF STACK CONNECTOR.

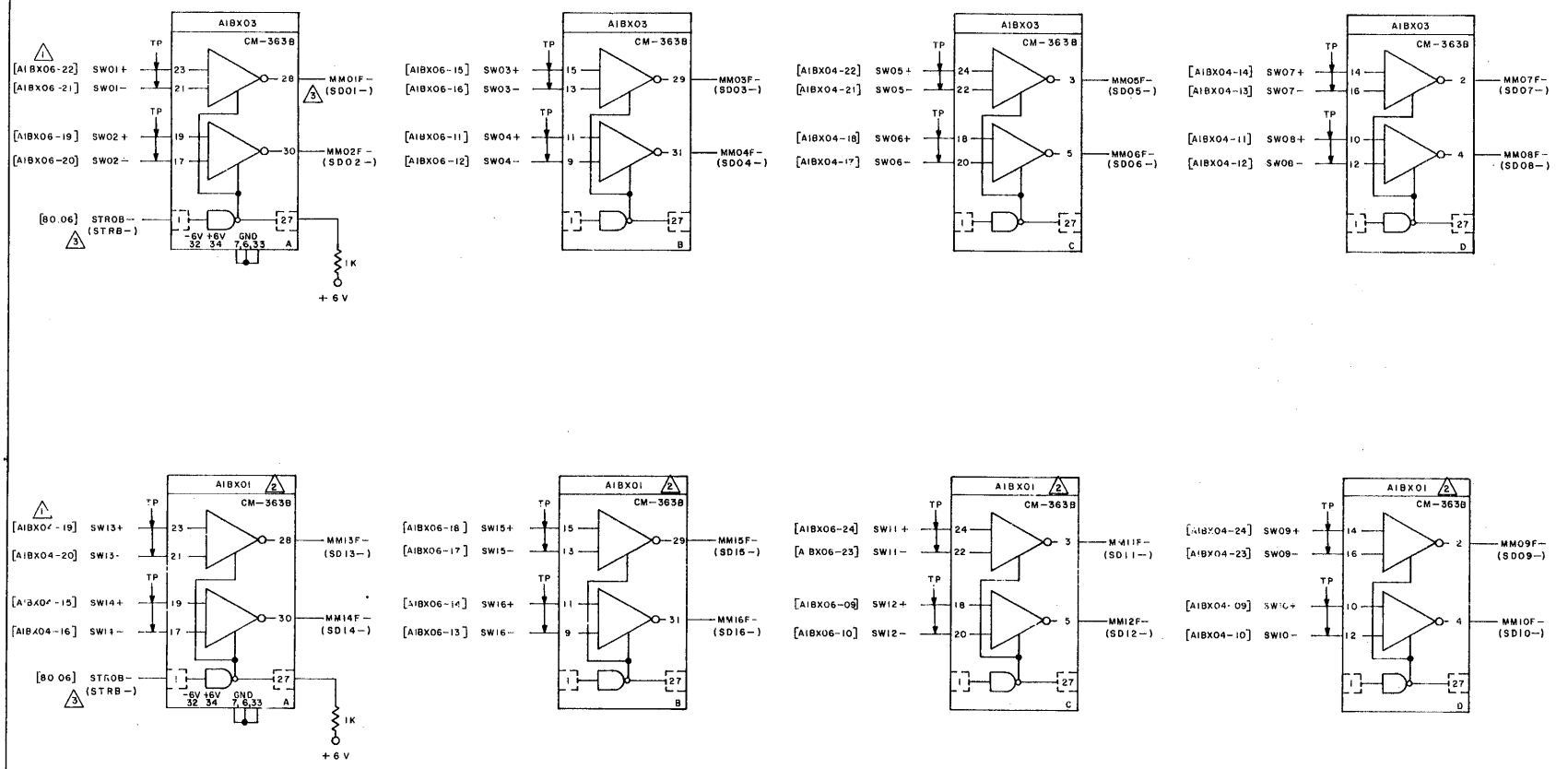
REVISIONS	REV.	
CHK.	A	TAKEN FROM SR. #54-3313
	B	ECO 9423
		EXT. CHGS SEE ECO 6/23/71 A.K.

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. D. HAMEL	DATE 1/21/69	
ENG. D. DAVIES	29-1-1969	
APP. C. Haase	2-12-1969	
PROJECT NO. 55202		

TITLE
CSM-160, ICM-160 AND
H-316 MEMORY X & Y SELECTION
DIODE MATRIX

SIZE C | DWG NO. 70022837 | RFV. B



NOTES:

1. A1BX04 & A1BX06 ARE CORE STACK CONNECTOR LOCATIONS.
2. THIS PAC NOT USED ON 8 BIT MODULES. THIS PAC REPLACED BY CM-469B ON 12 BIT MODULES.
3. CSM-160 AND ICM-160 NOMENCLATURE IN PARENTHESIS.

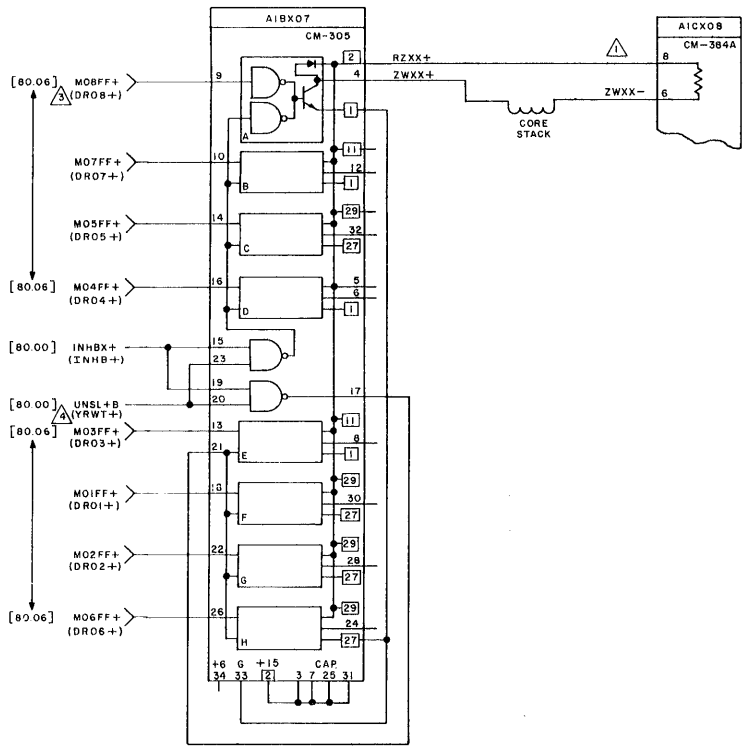
REV.	REVISIONS	CHK
A	TAKEN FROM R. 54-33.3	
B	ECO 7402 EXT CHANGES PB SEE ECO 10/13/69	
C	ECO 9423 EXT. CHGS SEE ECO A.K. 6/24/71	
D	ECO 10260 SEE ECO S.S.R. 3/22/72	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

DR.	D. HAMEL	DATE 1/27/69
ENG.	D. DAVIES	1-27-1969
APP.	[signature]	2-12-1969
PROJECT NO.	55202	

TITLE
CSM-160, ICM-160 AND H-316 MEMORY SENSE AMPLIFIERS

SIZE C | DWG NO. 70022838 | REV. D



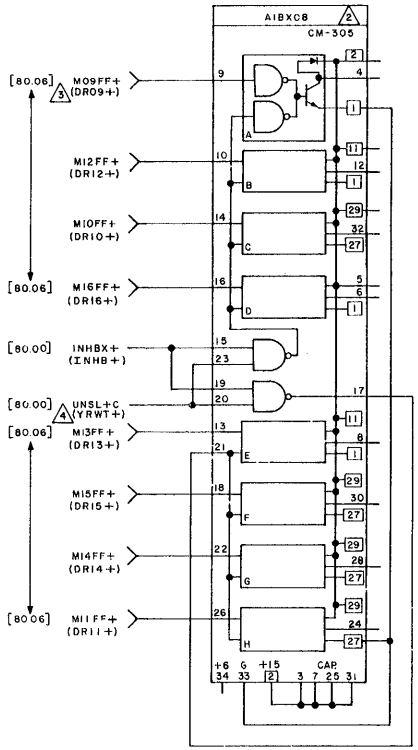


TABLE I

BIT XX	RZXX+		ZWXX+		ZWXX−	
	CM−305	CM−384A	CM−305	STACK	STACK	CM−384A
01	AIBX07−29	AICX08 −09	AIBX07−30	AICX06−01	AICX06−03	AICX08−05
02	29	11	28	AIBX06−31	AIBX06−32	03
03	11	15	08	AIBX06−02	AIBX06−01	19
04	05	14	06	AIAX06−29	AIAX06−31	02
05	—	—	32	AICX04−04	AICX04−02	07
06	—	—	24	AIBX04−31	AIBX04−32	01
07	11	10	12	AIBX04−02	AIBX04−01	04
08	AIBX07−02	08	AIBX07−04	AIAX04−32	AIAX04−30	06
09	AIBX08−02	20	AIBX08−04	AICX04−08	AICX04−06	30
10	29	23	32	AIAX04−28	AIAX04−26	31
11	—	—	24	AICX06−05	AICX06−07	27
12	11	13	12	AIAX06−25	AIAX06−27	21
13	11	26	08	AIBX04−29	AIBX04−30	28
14	—	—	28	AIBX04−04	AIBX04−03	29
15	29	17	30	AIBX06−29	AIBX06−30	25
16	AIBX08 05	AICX08 22	AIBX08−06	AIBX06−04	AIBX06−03	AICX08−32

NOTES:

1. TYPICAL CONNECTIONS FOR INHIBIT DRIVERS. TABLE I SHOWS CORRECT PIN LOCATIONS FOR BITS 1 THRU 16
2. THIS PAC NOT USED ON 8 BIT MODULES. THIS PAC REPLACED BY CM−488 ON 12 BIT MODULES.
3. ICM−160 AND CSM−160 NOMENCLATURE IN PARENTHESIS.
4. ICM−160 NOMENCLATURE.

REV.	REVISIONS	CHK
A	T AKEN FROM S.N. 54-333	
B	ECO R-6872 EXT CHANGES P B SEE ECO 5/27/69	
C	ECO 7402 EXT CHANGES SEE ECO 10/13/69	
D	ECO 9423 EXT. CHGS SEE ECO 6/24/71 A.K.	
E	ECO 9650 EXT. CHGS SEE ECO 7/22/71 A.K.	

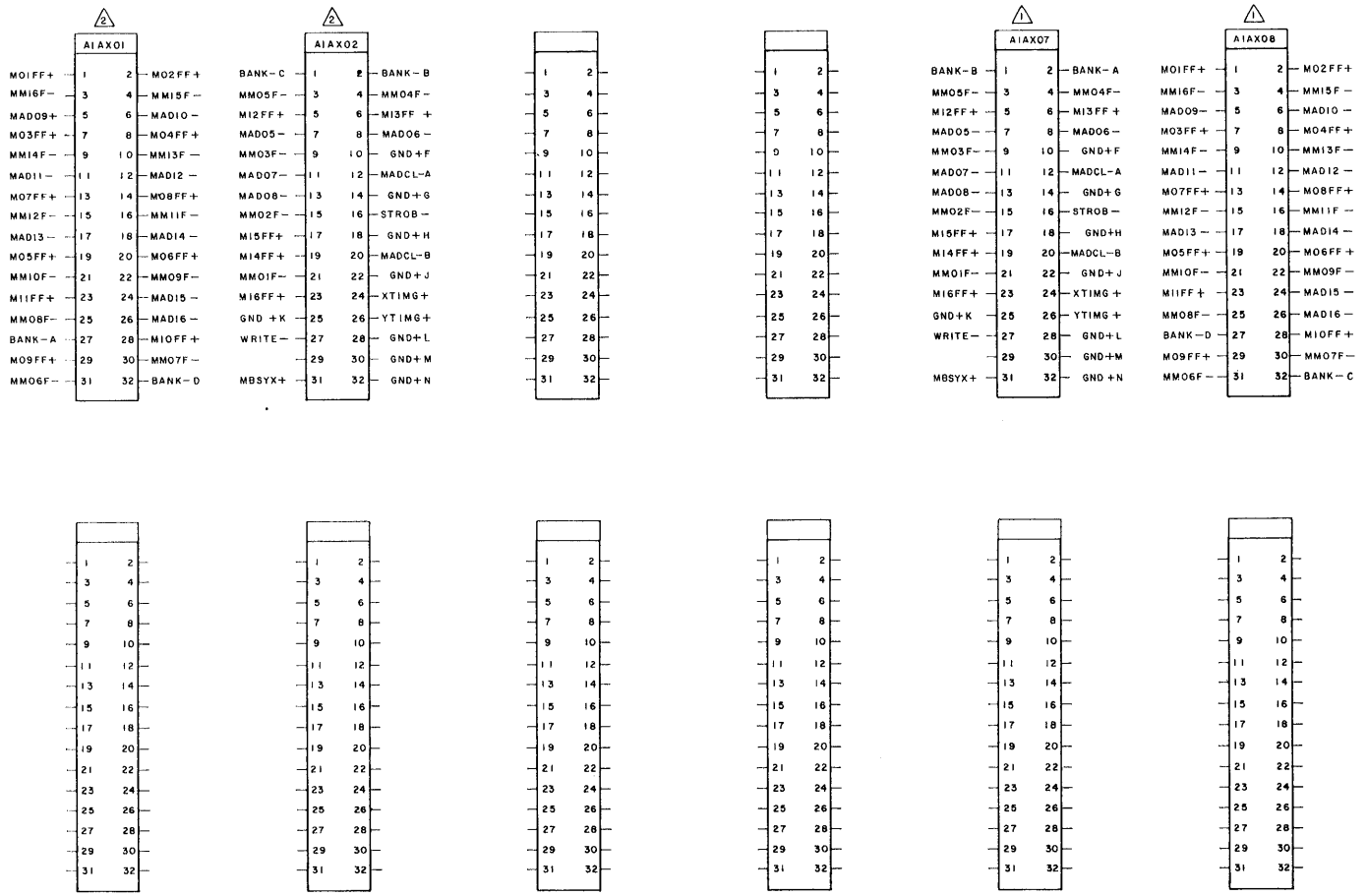
HONEYWELL INC
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

DR. D. HAMEL	DATE 1/30/67	
ENG. D DAVIES	1-30-1968	
APP. C Hause	2-12-1969	
PROJECT NO. 55202		

TITLE
CSM−160, ICM−160 AND H−316 MEMORY INHIBIT DRIVERS

SIZE C | DWG NO. 70022839 | REV. E

L.B.D. NO. 80.06



NOTES:

1. INPUT CABLE CONNECTORS (CE-020)
2. INTER-MODULE CONNECTORS. (DWG. A014998)

REV.	REVISIONS	CHK
A	TAKEN FROM S.R. S4-3313	
B	ECO 7402 EXT CHANGES P B SEE ECO 10/13/69	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

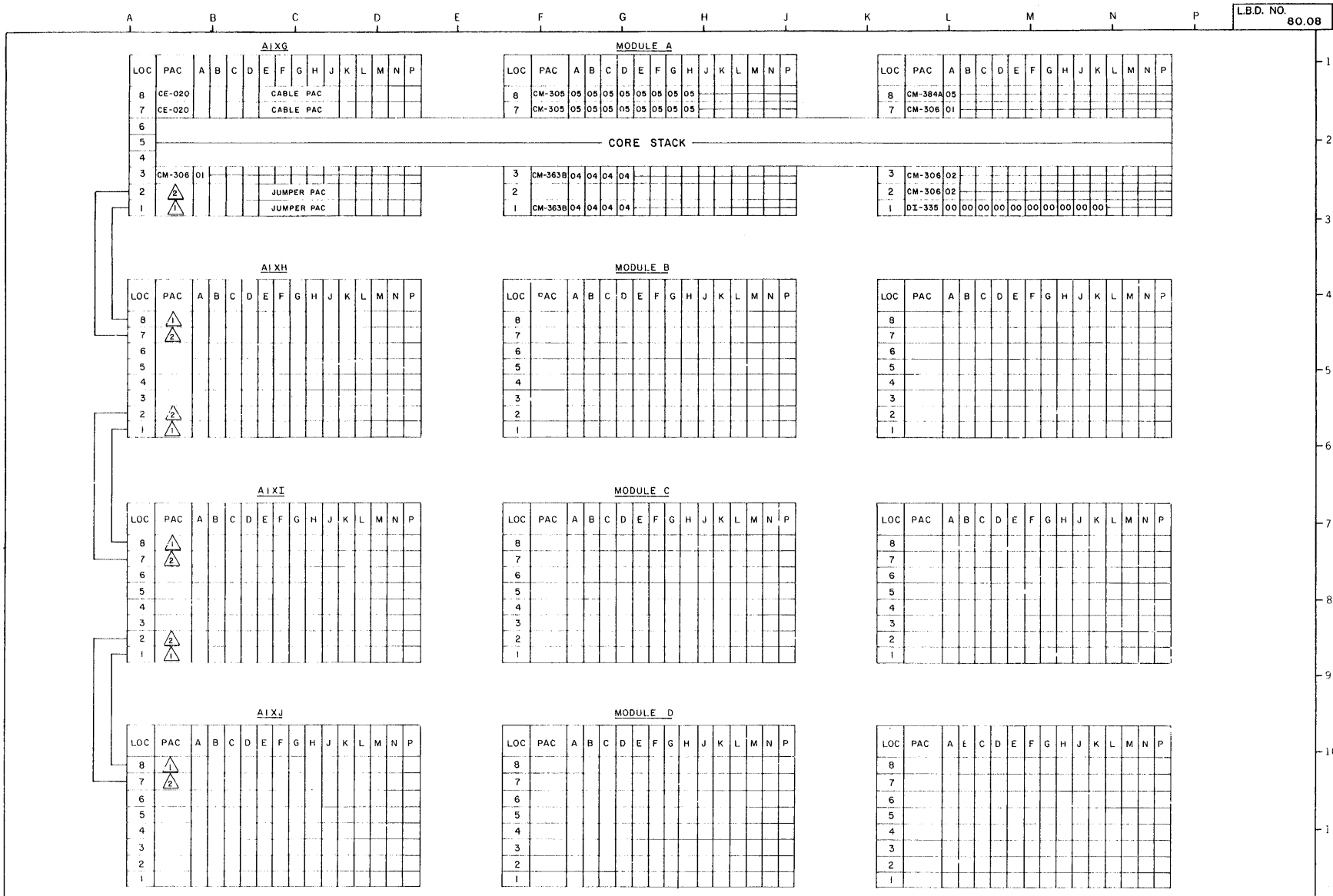
DR.	D. HAMEL	DATE 1/21/69
ENG.	D. DAVIES	1-29-1969
APP.	C. Haas	2-12-1969
PROJECT NO.	55202	

TITLE
H-316 MEMORY
1X3 CONN. WIRING

SIZE C | DWG NO. 70022840 | REV. B

F2011-1068

L.B.D. NO. 80.08



NOTES:

1. JUMPER PAC A01499701 } USED FOR MULTI-MODULE CONNECTIONS.
2. JUMPER PAC A01499702 }
3. PAC LOCATIONS FOR ALL MODULES THE SAME AS MODULE "A" WITH THE EXCEPTION OF 1 & 2

CHK	REVISIONS	REV.
	TAKEN FROM SR 54 393	A
MK	ECO 7690 EXT CHANGES SEE ECO 1/2/70 A.K.	B
	ECO 8356 EXT. CHGS SEE ECO 5/18/70 A.K.	C
	ECO 10260 SEE ECO 3/22/72 S.S.R.	D

HONEYWELL INC
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

DR. D. HAMEL	DATE	
ENG. K. IZBICKI	1-31-1969	
APP. E Haas	2-12-1969	
PROJECT NO. 55232		

TITLE
H-316 MEMORY
PAC COMP. & ALLOCATION

SIZE C | DWG NO. 70022841 | REV. D

P70022841 PARTS LIST

SAFETY WIRING

H316 Memory PAC Complement

Part Number	Description	Quantity
70 006 707 701	NAND Type 1 PAC, Model DI-335	1
70 021 896 701	Selector μ-PAC, Model CM-306	4
70 022 970 702	Resistor μ-PAC, Model CM-384A	1
70 022 955 707	Sense Amplifier μ-PAC, Model CM-363B	2
70 021 402 701	Inhibit μ-PAC, Model CM-305	2
70 942 507 002	Core Memory Unit, Plugable	1

SECTION 5
MEMORY PAC DESCRIPTIONS

This section contains the following circuit descriptions and parts lists for the special μ-PACs used in the H316 Magnetic Core Memory Modules.

CM-305/CM-488	Inhibit PAC
CM-306/CM-640	Selector PAC
CM-363A/CM-489A/ CM-734/CM-735	Sense Amplifier PAC
CM-363B/CM-489B/ CM-734/CN-735	Sense Amplifier PAC
CM-384A	Resistor PAC
DI-335	NAND Type 1 PAC
XP-330	Extender PAC

INHIBIT μ-PAC, MODELS CM-305/CM-488

The Inhibit μ-PAC, Model CM-305 (Figure 1 and 2), contains two groups of four 425 mA transistor switches and one NAND gate. Each switch is controlled by a data input and strobed by a common line within each circuit.

An output switch is turned on (active state) when the corresponding data input is at an active state, the timing input for circuits A, B, C and D is at a passive state, and the timing input for circuits E, F, G, and H is at an active state.

The emitters of the output transistors are brought out to external pins 1 and 27. Optional capacitors C1, C2, and C3 are provided for filtering the +15V supply. Clamp diodes at each collector are used with inductive loads.

The CM-488 contains one group of four transistor switches. Circuits D, E, F, and G of Figure 1 and 2 are omitted.

Specifications

Frequency of Operation

DC to 2 MHz

Input Loading

1 unit load each (1.6 mA)

Output Characteristics

Current: 425 mA (max)
Voltage: 17.5V (max)
Power: 200 mW (max)

Current Requirements

+6V: 70 mA (max)

Circuit Delay (420 mA Resistive Load)

Turn-on Delay (1.5V of input to 10% of current)	190 ns (max)
Turn-off Delay (1.5V of input to 90% of current)	190 ns (max)

Power Dissipation

2.2W (max)

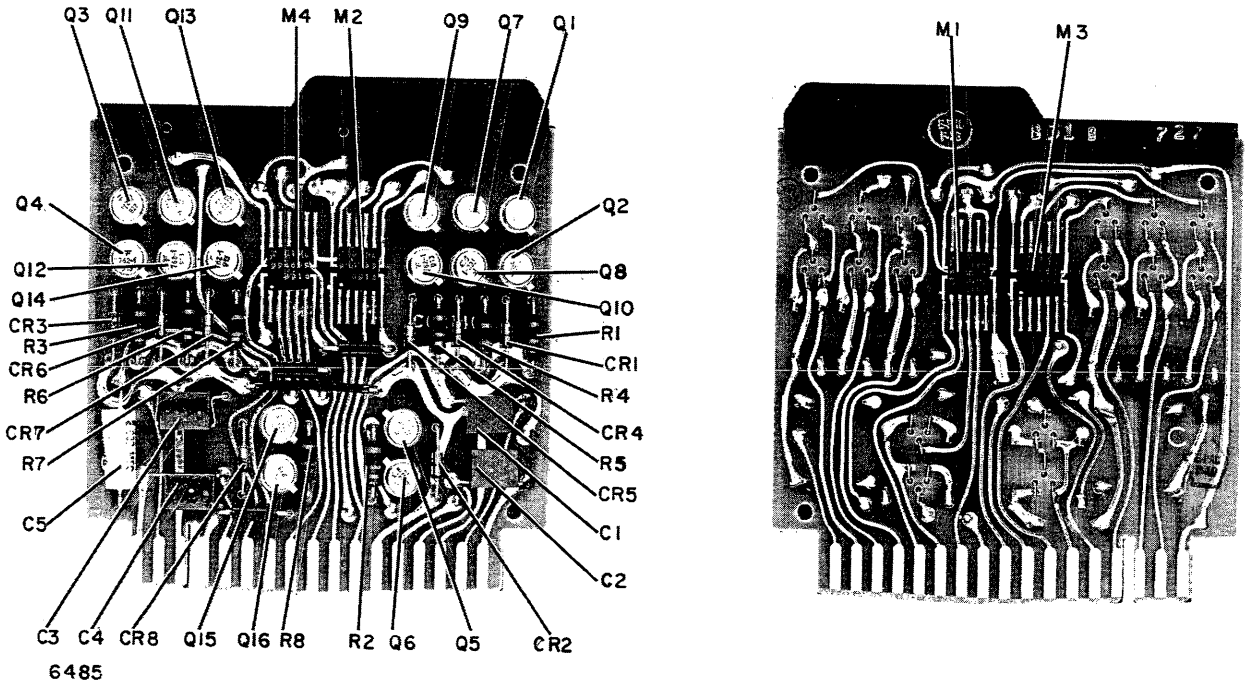


Figure 1. Inhibit μ-PAC, Models CM-305/CM-488, Parts Location (Dwg B70021402, Rev. D)

Electrical Parts List (No. P70021402, Rev. E)

Ref. Desig.	Description	Part No.
C1-C4	CAPACITOR, FIXED, SOLID TANTALUM: 6.8 μF ±20%, 20 Vdc	70 930 235 211
C5	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 20 Vdc	70 930 313 016
CR1-CR8--CR1-CR3, CR8*	DIODE, SILICON	70 943 083 003
M1	MICROCIRCUIT: Type 936, hex single-input inverter integrated circuit	70 950 105 004
M2-M4--M4*	MICROCRICUIT: Type 946, quad two-input NAND gate integrated circuit	70 950 105 002
Q1, Q3, Q5, Q7, Q7, Q9, Q11, Q13, Q15--Q1, Q3, Q5, Q15*	TRANSISTOR: Silicon NPN	70 943 722 002
Q2, Q4, Q6, Q8, Q10, Q12, Q14, Q16--Q2, Q4, Q6, Q16*	TRANSISTOR: Silicon NPN Type 778-2	70 943 778 002
R1-R8--R1-R3, R8*	RESISTOR, FIXED, COMPOSITION: 100 ohms ±5%, 1/4W	70 932 007 025

*CM-488 only

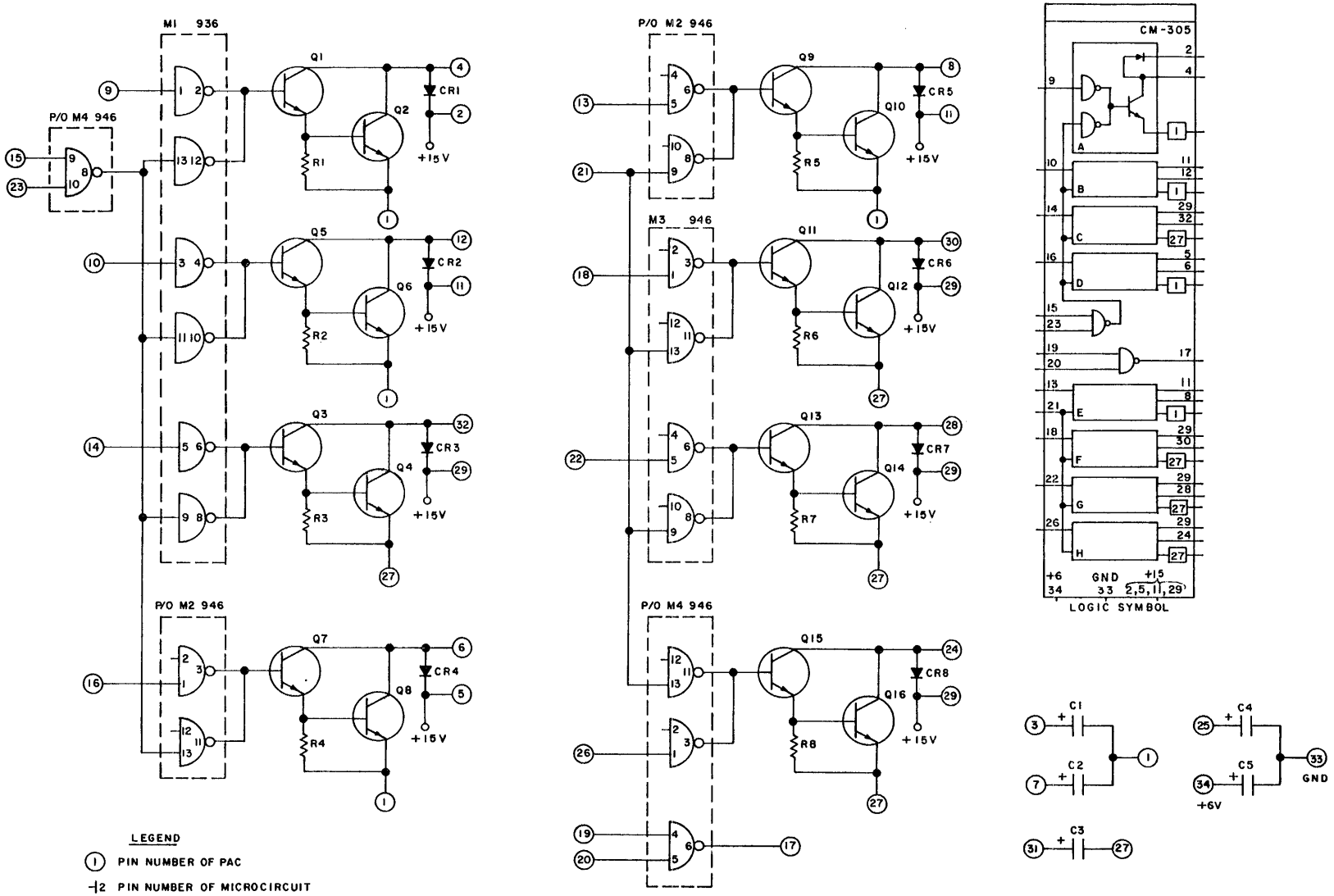


Figure 2. Inhibit μ-PAC, Models CM-305/CM-488, Schematic Diagram and Logic Symbol (Dwg B70021402, Rev. D)

SELECTOR μ-PAC, MODELS CM-306/CM-640

The Selector μ-PAC, Model CM-306 (Figures 1 and 2), contains three registers, as well as decoding and drive circuitry for half of an 8 x 8 selection matrix. The outputs can sink or switch inductive loads of up to 450 mA with voltages up to +17V.

The CM-640 is identical to the CM-306 except the address gates are connected as buffers rather than register stages.

Address Circuits

Three Type 961 power amplifier gates constitute the three register stages of the CM-306. Pin 6 is a common reset input to all three register stages. Pins 3, 14, and 20 are set inputs; pins 8, 9, and 17 are reset inputs; pins 10, 16, and 22 are set outputs. One type 961 gate serves as an address buffer. Five type 961 gates serve as address buffers for the CM-640.

Decoding and Drive Circuitry

Four F-33 flat packs decode the address circuit inputs and sink or switch up to 450 mA of current into inductive loads. Input pin 24 at logic ONE enables the switch outputs. Pins 25 and 28 are inputs to a NAND gate whose output, at logic ONE, activates the sink outputs. Only one output (sink or switch) of an F-33 can be activated during a given cycle.

The expansion input, pin 4, must be at logic ONE to enable the CM-306 μ-PAC.

Input and Output Signals

Table 1 lists logic levels on various pins and the resulting active outputs.

Table 1
Input/Output Logic Signals

Pin 20 (A3+)	Pin 14 (A2+)	Pin 3 (A1+)	Pin 24 (Timing Switch)	Pins 25 and 28 (Timing Sink)	Active Output Pin No.
0	0	0	0	1	11
0	0	0	1	0	13
0	0	1	0	1	18
0	0	1	1	0	15
0	1	0	0	1	27
0	1	0	1	0	30
0	1	1	0	1	31
0	1	1	1	0	32
1	0	0	0	1	1
1	0	0	1	0	5
1	0	1	0	1	12
1	0	1	1	0	7
1	1	0	0	1	19
1	1	0	1	0	21
1	1	1	0	1	26
1	1	1	1	0	23

Specifications

Input Loading

Address Inputs	1 unit load
Reset Input	3 unit loads
Expansion Input	6 unit loads
Timing Inputs	1 unit load

Output Characteristics

Current (sink or switch)	450 mA (max)
Voltage (sink or switch)	17V (max)
Power (sink or switch)	560 mW (max)
Collector-Emitter Saturation Voltage (sink or switch)	0.9V (max)
Register Set Output	4 unit loads

Circuit Delay (430 mA Resistive Load)

Turn-on Delay (1.5V of timing input to 90% of current)	Sink	120 ns (max)
	Switch	140 ns (max)
Turn-off Delay (1.5V of timing input to 10% of current)	Sink	200 ns (max)
	Switch	120 ns (max)

Current Requirements

100 mA at 15V
45 mA at +6V

Power Dissipation

2.5W (max)

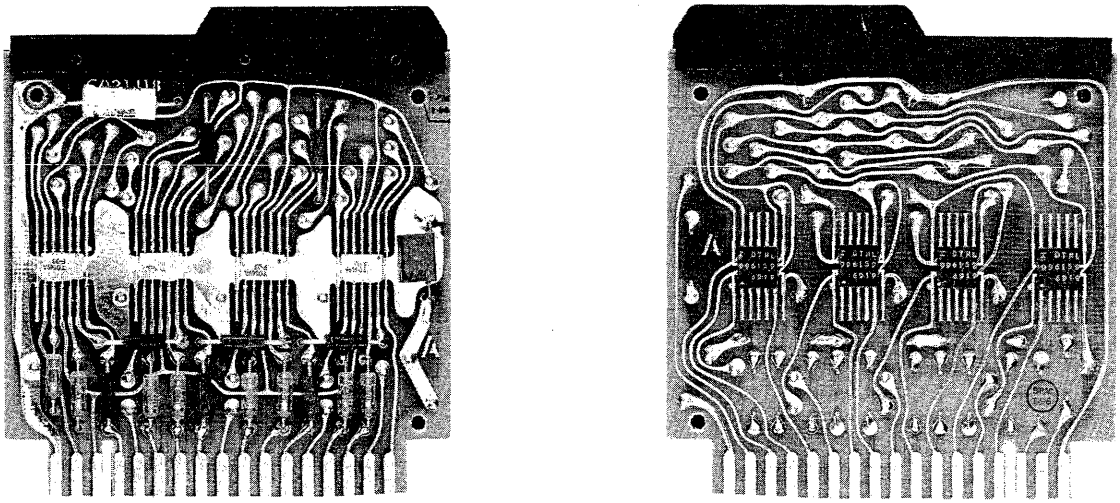


Figure 1. Selector μ-PAC, Model CM-306/CM-640, Parts Location (Dwg B70021896, Rev. D)

Electrical Parts List (No. P70021896, Rev. D)

Ref. Desig.	Description	Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 016
C2	CAPACITOR, FIXED, SOLID TANTALUM: 6.8 μF ±20%, 20 Vdc	70 930 235 211
CR1-CR8	DIODE, SILICON	70 943 083 003
M1-M4	MICROCIRCUIT: Type 961, dual four-input NAND integrated circuit	70 950 105 009
M5-M8	MICROCIRCUIT: F-33, selection switch integrated circuit	70 950 100 033

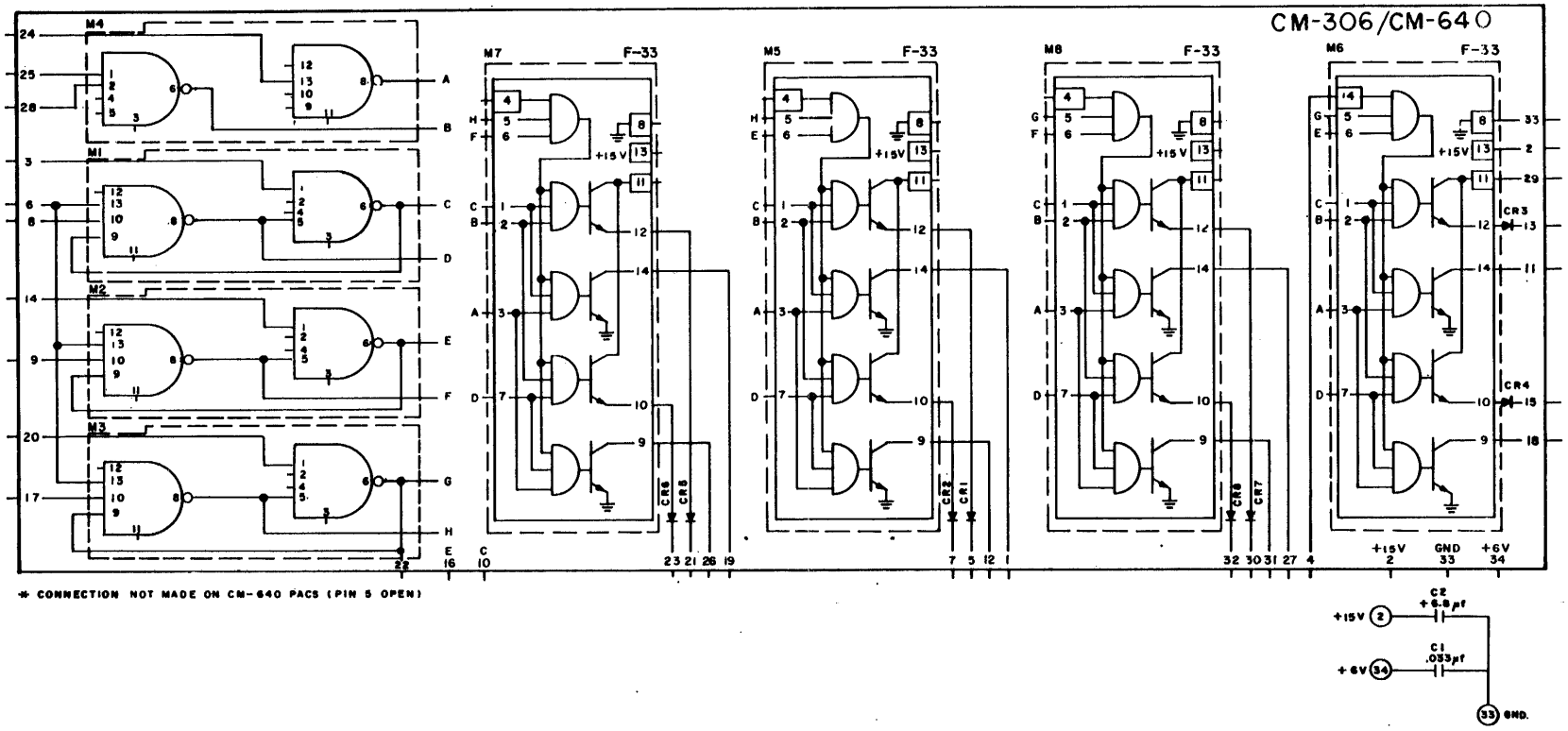


Figure 2. Selector μ-PAC, Model CM-306,
Schematic Diagram and Logic Symbol
(Dwg B70021896, Rev. D)

SENSE AMPLIFIER μ-PAC, MODELS CM-363A/CM-489A/CM-734/CM-735

The Sense Amplifier μ-PAC, Models CM-363A and CM-734, contains four dual-in-line integrated circuit sense amplifiers, each of which contains two complete amplifier circuits capable of detecting and amplifying core signals. Each circuit has its own strobe input, all inputs being driven by the same buffer amplifier. A resistor divider network determines the threshold voltage for the eight circuits. Each amplifier output is connected to an inverter gate. The μ-PAC also contains the sense line termination resistors for each circuit.

The CM-489A and CM-735 contain only two dual-in-line integrated circuit sense amplifiers. Circuits A and B are omitted.

Circuit Function

A differential signal which is greater than the threshold voltage will produce a positive sense amplifier output if the strobe circuit is enabled. A negative strobe signal applied to the strobe buffer amplifier will enable the strobe gate and a positive signal will disable it. The sense amplifier output will be inverted, making a negative signal available to perform a logical OR function.

Specifications

Strobe Input

Input loading: 1.6 mA

DC Threshold

14 mV to 28 mV

Current Requirements

+6V: 332 mA (max)
-6V: 110 mA (max)

Power Dissipation

2.7W (max)

Output

Delay from strobe input to PAC output

Leading edge: 155 ns (max)
Trailing edge: 155 ns (max)

Pulse width with 100 ns sense input
pulse width: 80 ns (min)
Drive capability: 12.8 mA

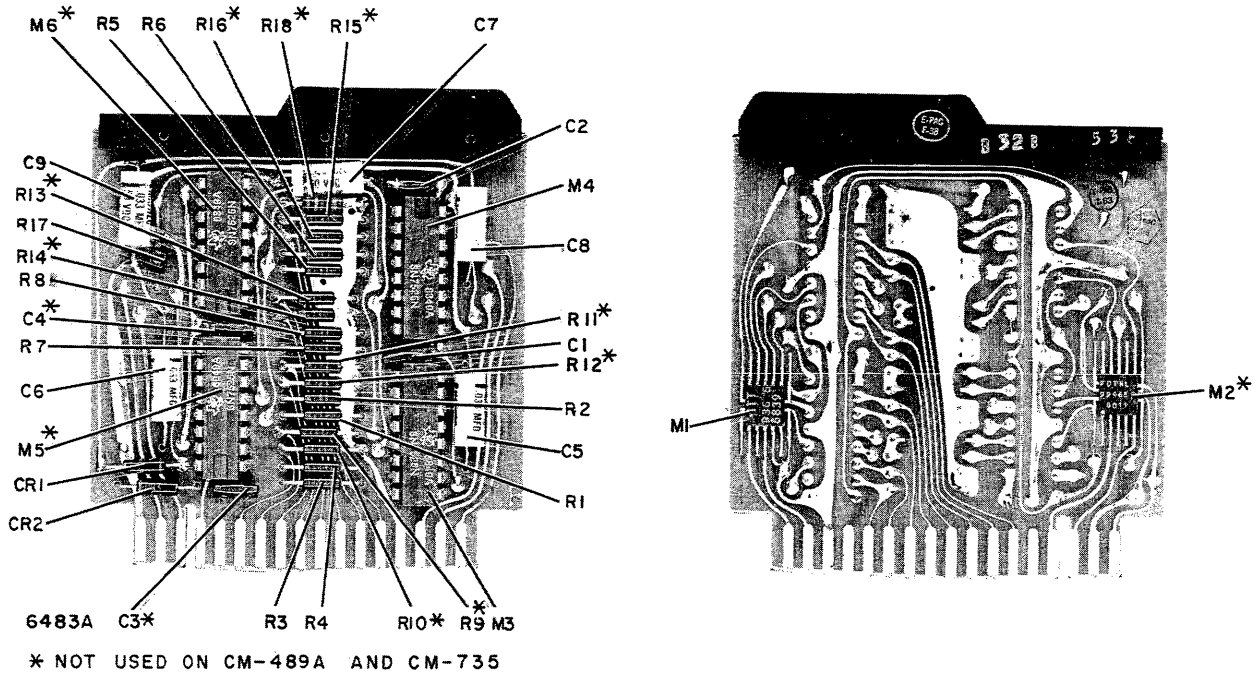


Figure 1. Sense Amplifier μ-PAC, Models CM-363A/CM-489A, CM-734/CM-735, Parts Locations (Dwg No. A70022955, Rev. E)

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C4	CAPACITOR, FIXED, MICA DIELECTRIC: 120 pF ±10%, 100 Vdc	70 930 016 030
C5-C9	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 021
CR1, CR2	DIODE, SILICON	70 943 083 002
M1	MICROCIRCUIT: Type 936, hex inverter integrated circuit	70 950 105 004
M2	MICROCIRCUIT: Type 946, quad two-input NAND gate integrated circuit	70 950 105 002
M3-M6[1,2] M3, M4[2]	MICROCIRCUIT: Dual sense amplifier integrated circuit (See note 5)	70 950 100 XXX
M3-M6[3,4] M3, M4[4]	MICROCIRCUIT: Dual sense amplifier integrated circuit	70 950 100 042
R1-R16	RESISTOR, FIXED, FILM: 150 ohms ±2%, 1/4W	70 932 114 029
R17	RESISTOR, FIXED, FILM: 270 ohms ±2%, 1/4W	70 932 114 035
R18	RESISTOR, FIXED, FILM: 1 ohm ±2%, 1/4W	70 932 114 145
	[1]CM-363/CM-363A [2]CM-489/CM-489A [3]CM-734 [4]CM-735 [5]Part No. 70 950 100 034 (plastic) may be used interchangeably with 70 950 100 042 (ceramic)	

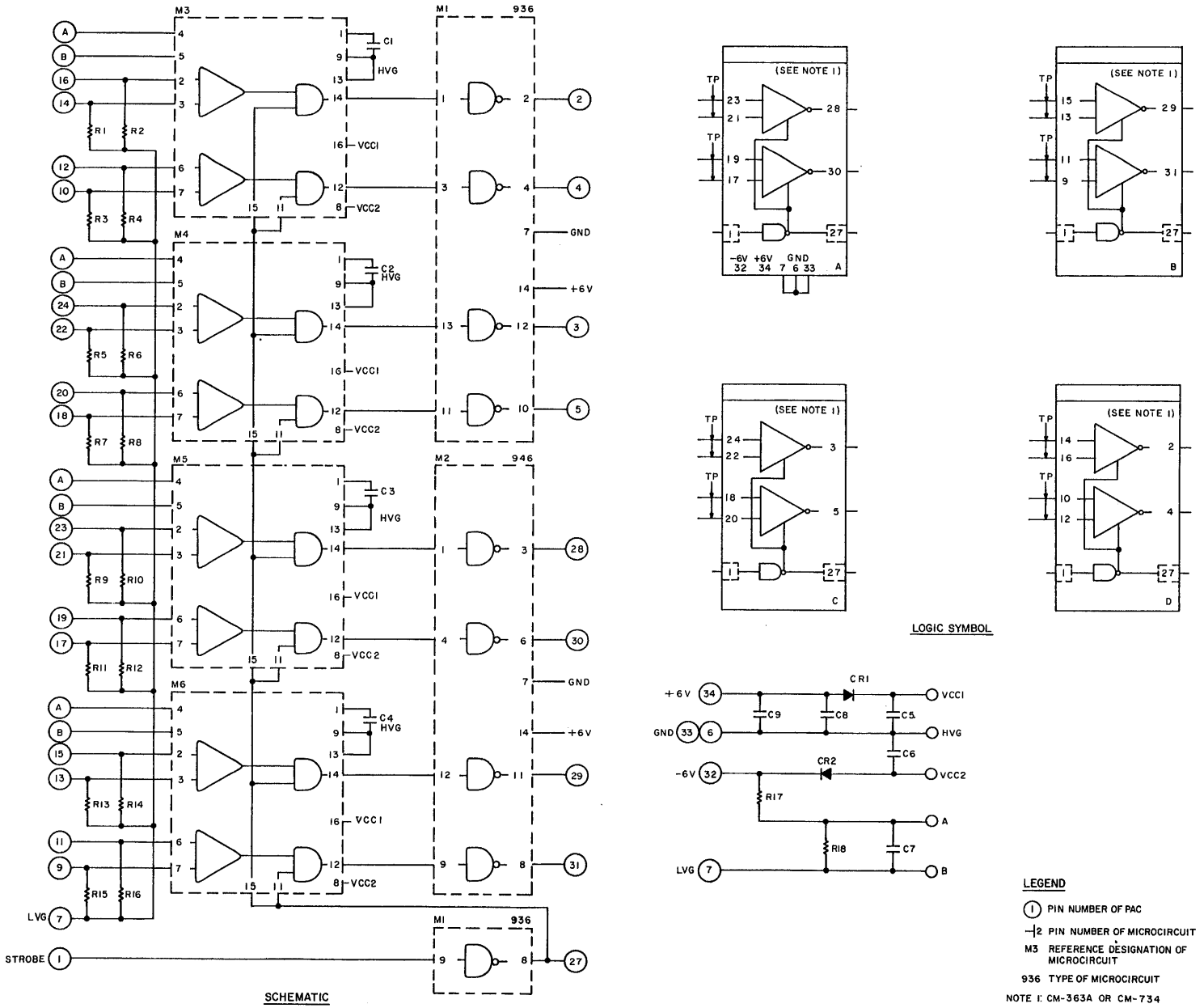


Figure 2. Sense Amplifier μ-PAC, Models CM-363A/CM-734, Schematic Diagram and Logic Symbol (Dwg A70022955, Rev. E)

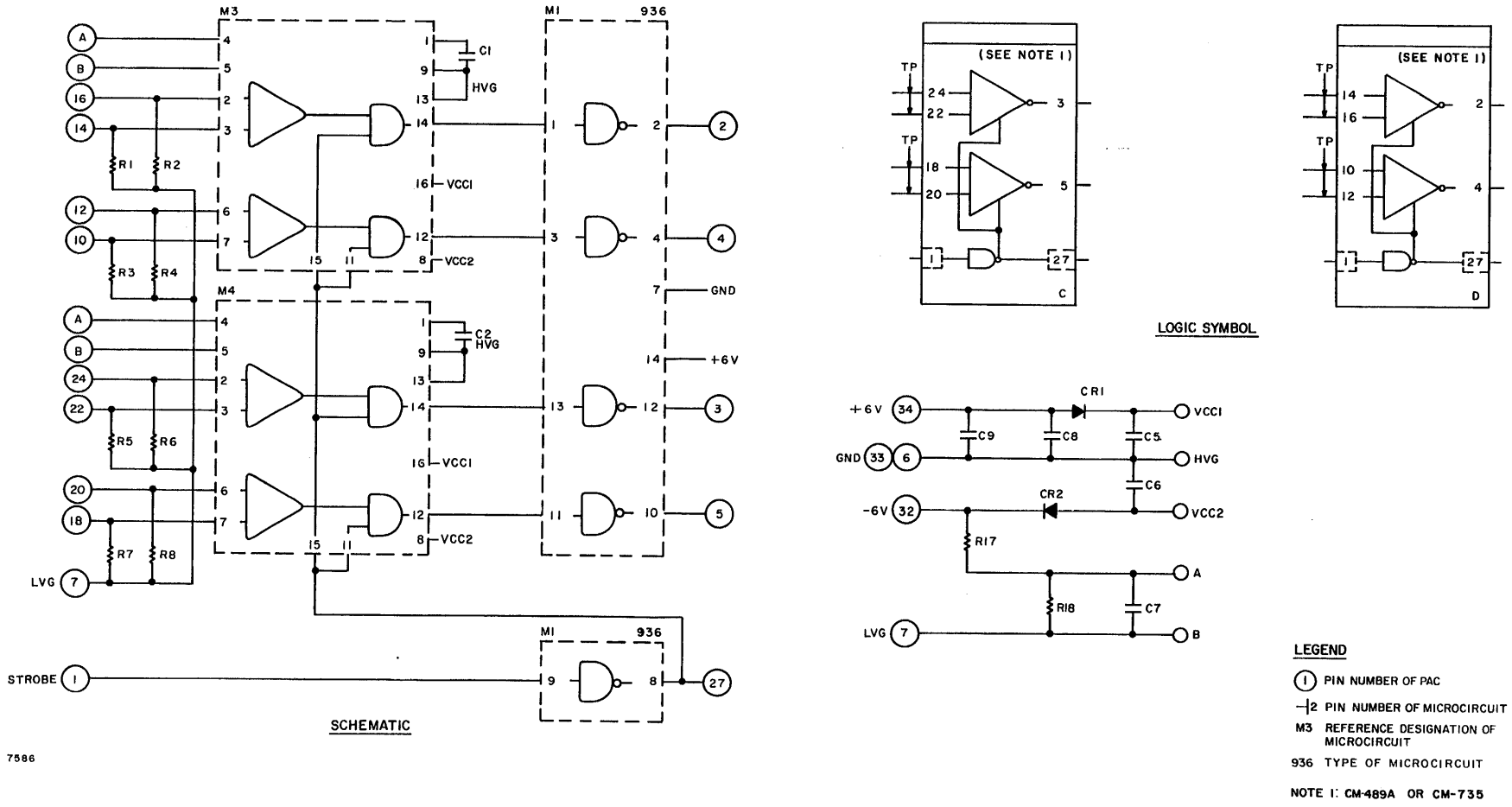


Figure 3. Sense Amplifier μ-PAC, Models CM-489A/CM-735, Schematic Diagram and Logic Symbol (Dwg A70022955, Rev E)

SENSE AMPLIFIER μ-PAC, MODELS CM-363B/489B/734/735

The Sense Amplifier μ-PAC, Models CM-363B and CM-734, contains four dual-in-line integrated circuit sense amplifiers, each of which contains two complete amplifier circuits capable of detecting and amplifying core signals. Each circuit has its own strobe input, all inputs being driven by the same buffer amplifier. A resistor divider network determines the threshold voltage for the eight circuits. Each amplifier output is connected to an inverter gate. The μ-PAC also contains the sense line termination resistors for each circuit.

The CM-489B and CM-735 contain only two dual-in-line integrated circuit sense amplifiers. Circuits A and B are omitted.

Circuit Function

A differential signal which is greater than the threshold voltage will produce a positive sense amplifier output if the strobe circuit is enabled. A negative strobe signal applied to the strobe buffer amplifier will enable the strobe gate and a positive signal will disable it. The sense amplifier output will be inverted, making a negative signal available to perform a logical OR function.

Specifications

Strobe Input

Input loading: 1.6 mA

DC Threshold

14 mV to 28 mV

Current Requirements

+6V: 332 mA (max)
-6V: 110 mA (max)

Power Dissipation

2.7W (max)

Output

Delay from strobe input to PAC output

Leading edge: 155 ns (max)
Trailing edge: 155 ns (max)

Pulse width with 100 ns sense input pulse width: 80 ns (min)
Drive capability: 12.8 mA

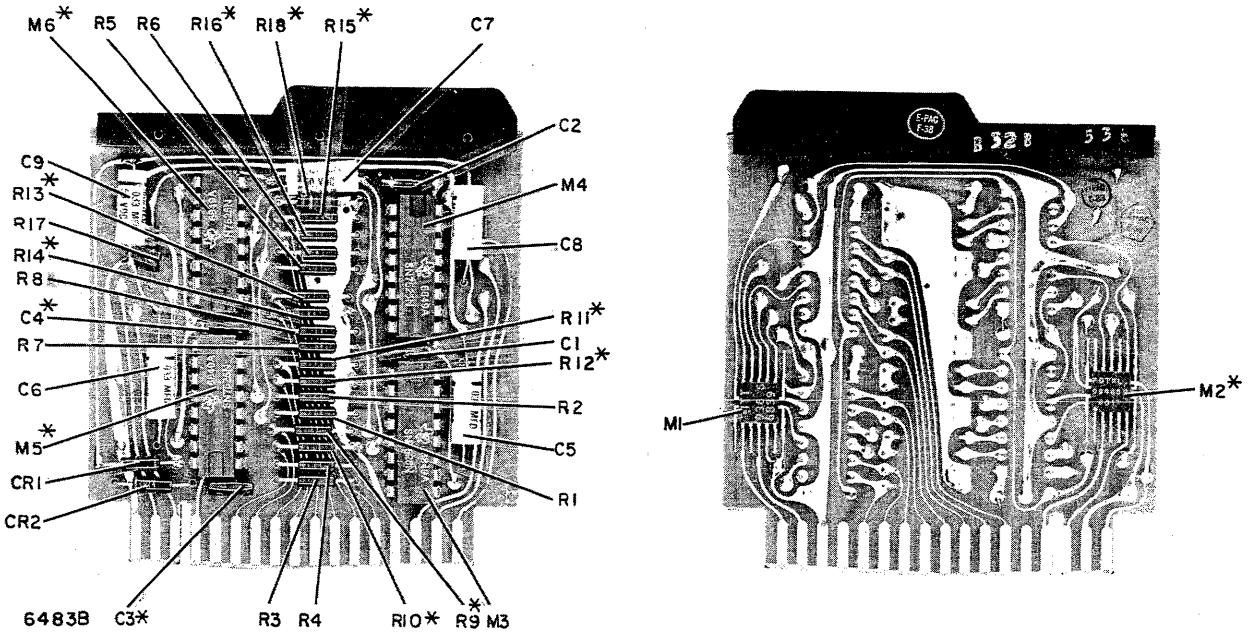


Figure 1. Sense Amplifier μ-PAC, Models CM-363B/489B/734/735, Parts Locations (Dwg No. A70022955, Rev. F)

Electrical Parts List

Ref. Desig.	Description	Part No.
C1-C4	CAPACITOR, FIXED, MICA DIELECTRIC: 120 pF ±10%, 100 Vdc	70 930 016 030
C5-C9	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	70 930 313 021
CR1, CR2	DIODE, SILICON	70 943 083 002
M1	MICROCIRCUIT: Type 936, hex inverter integrated circuit	70 950 105 004
M2	MICROCIRCUIT: Type 946, quad two-input NAND gate integrated circuit	70 950 105 002
M3-M6[1] M3, M4[2]	MICROCIRCUIT: Dual sense amplifier integrated circuit (See note 5)	70 950 100 XXX
M3-M6[3] M3, M4[4]	MICROCIRCUIT: Dual sense amplifier integrated circuit	70 950 100 042
R1-R16	RESISTOR, FIXED, FILM: 150 ohms ±2%, 1/4W	70 932 114 029
R17	RESISTOR, FIXED, FILM: 270 ohms ±2%, 1/4W	70 932 114 035
R18	RESISTOR, FIXED, FILM: 1 ohm ±2%, 1/4W	70 932 114 145
	[1]CM-363B [2]CM-489B [3]CM-734 [4]CM-735 [5]Part No. 70 950 100 034 (plastic) may be used interchangeably with 70 950 100 042 (ceramic)	

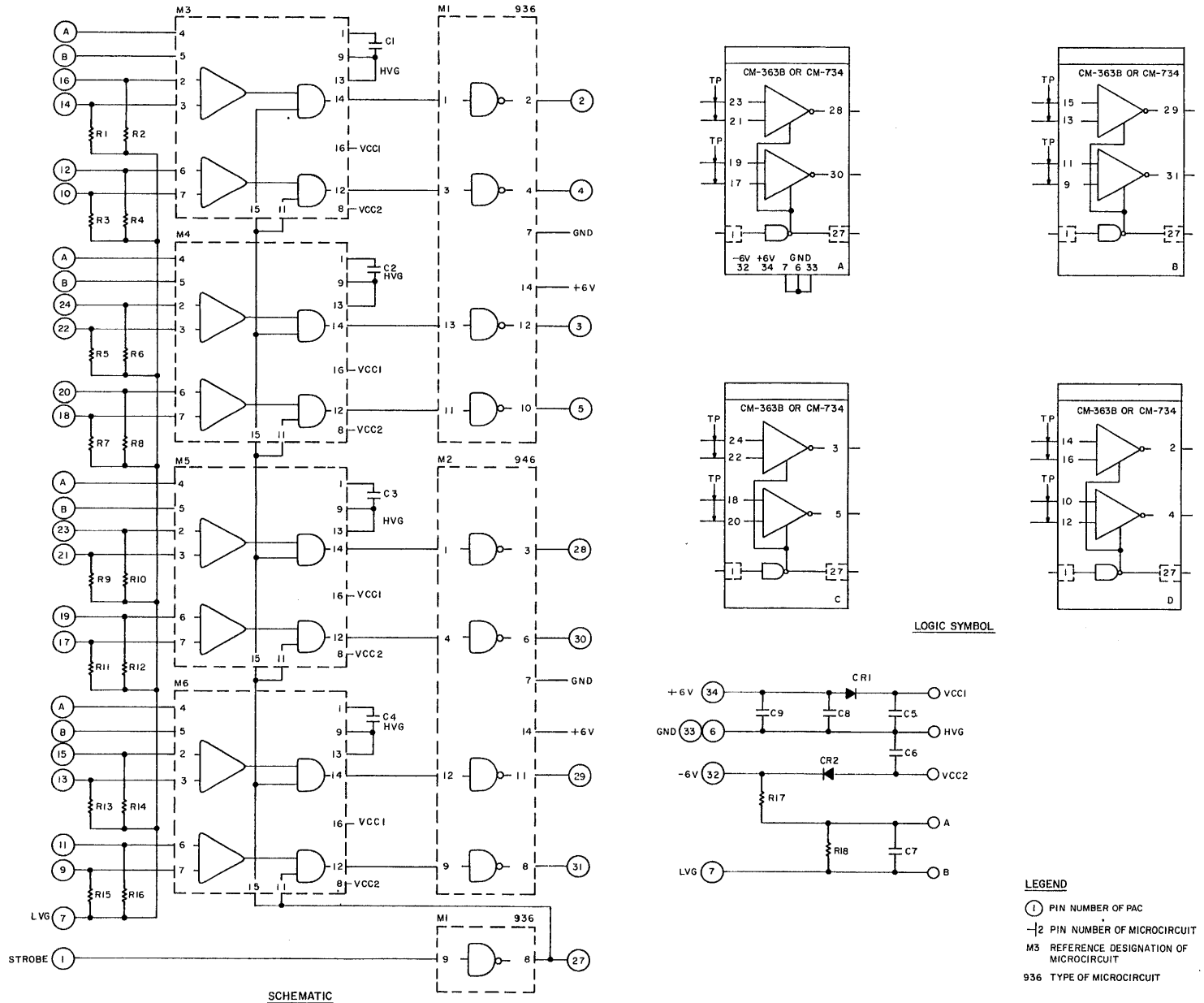


Figure 2. Sense Amplifier μ-PAC, Models CM-363B/734, Schematic Diagram and Logic Symbol (Dwg No. A70022955, Rev. F)

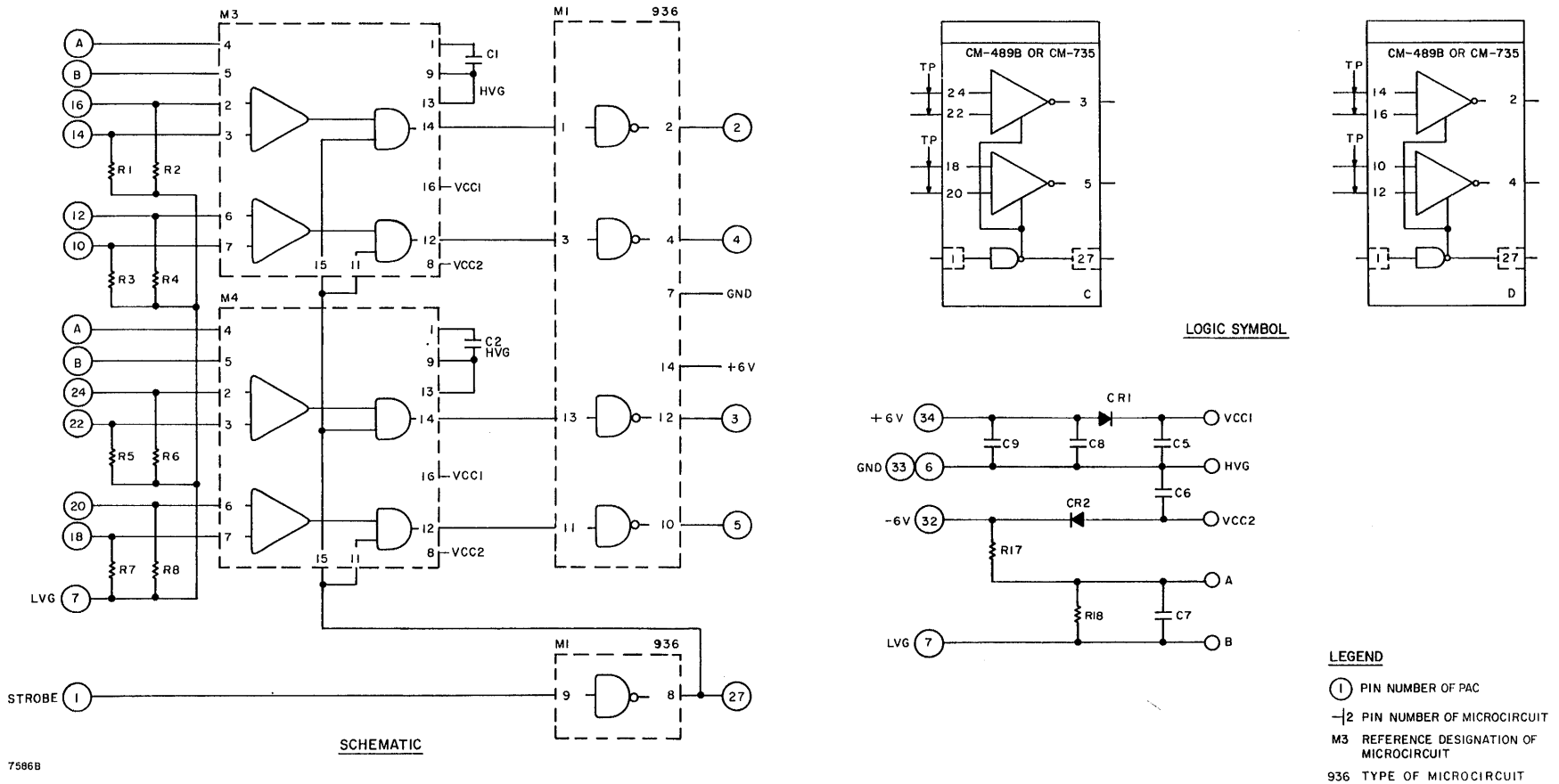


Figure 3. Sense Amplifier μ-PAC, Models CM-489B/735, Schematic Diagram and Logic Symbol (Dwg No. A70022955, Rev. F)

RESISTOR μ-PAC, MODEL CM-384A

The Resistor μ-PAC, Model CM-384A (Figures 1 and 2), contains 20 3W wirewound resistors. Sixteen of these (R1 through R16) are used as current limiting resistors for the inhibit drive lines. The four noninductive resistors form two groups of parallel pairs used as current-limiting resistors for the X- and Y- drive lines.

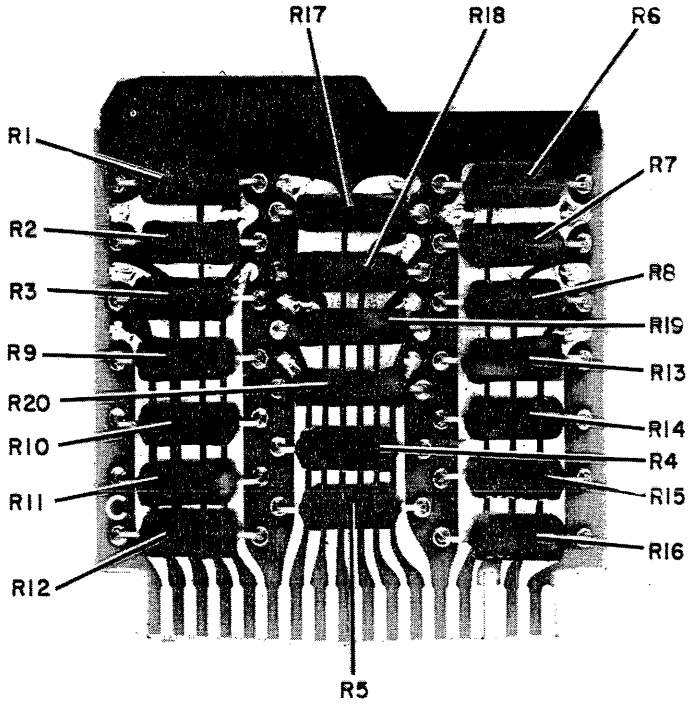
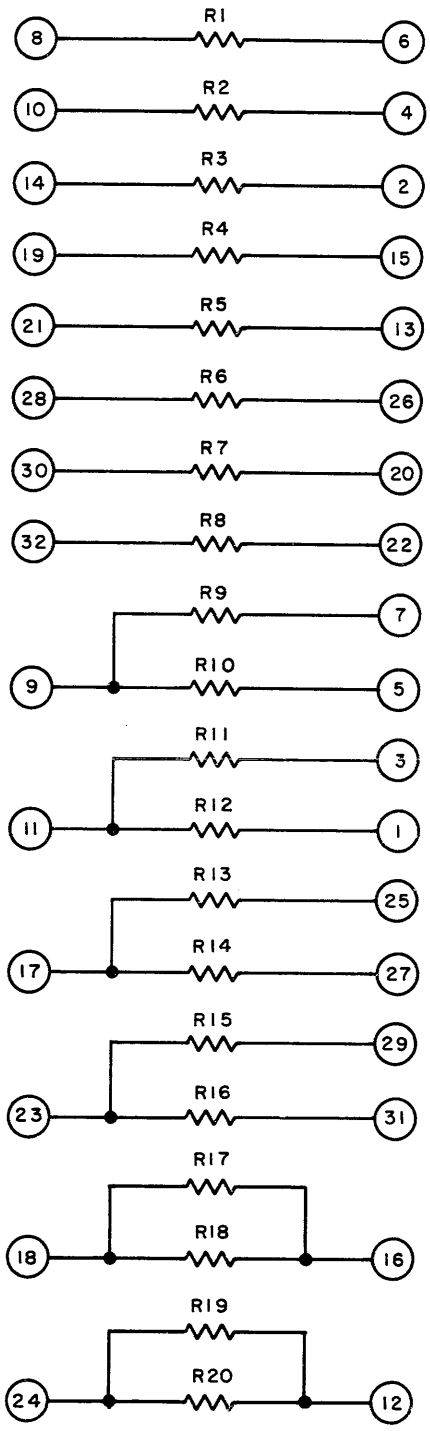


Figure 1. Resistor μ-PAC, Model CM-384A, Parts Locations (A70022970, Rev D)

Electrical Parts List (No. P70022970, Rev D)

Ref. Desig.	Description	Part No.
R1-R16	RESISTOR, FIXED, WIREWOUND: 30 ohms ±1%, 3W	70 932 206 409
R17	RESISTOR, FIXED, WIREWOUND: 60 ohms ±1%, 3W	70 932 223 123
R18-R20	RESISTOR, FIXED, WIREWOUND: 50 ohms ±1%, 3W	70 932 223 122



5942

Figure 2. Resistor μ-PAC, Model CM-384A, Schematic Diagram

NAND TYPE 1 PAC, MODEL DI-335

The NAND Type 1 PAC, Model DI-335 (Figures DI-335-1 and DI-335-2), contains 10 independent 2-input NAND gates. Each gate performs the NAND function for positive logic (+6V = ONE, 0V = ZERO). For negative logic, it becomes a NOR gate.

Two of the 10 gates have separate load connections available at the PAC terminals. Outputs of these gates can be tied together, using a single load resistor, without loss of output drive capability. A detailed description of the basic NAND circuit appears in Section 1.

INPUT AND OUTPUT SIGNALS

Inputs

When both inputs to a gate are +6V or not connected, the output is at ground. When any input is at ground, the output is +6V.

Load

This point is internally connected through a collector load resistor to +6V.

Collector Output

The collector output must be connected to at least one load resistor, either internal or external to the module.

Output

Each output terminal is internally connected to a collector load resistor. If an output is connected to load points or other outputs, the output drive capability of the structure is reduced.

SPECIFICATIONS

Frequency of Operation (System)

DC to 5 MHz

Input Loading

1 unit load each

Fan-In

Refer to Section 1

Output Drive Capability

8 unit loads each

Outputs in Parallel

Refer to Section 1

Circuit Delay

(Measured at +1.5V, averaged over two stages)
30 ns (max)

Current Requirements

+6V: 112 mA (max)

Power Dissipation

0.67W (max)

Handle Color Code

Red

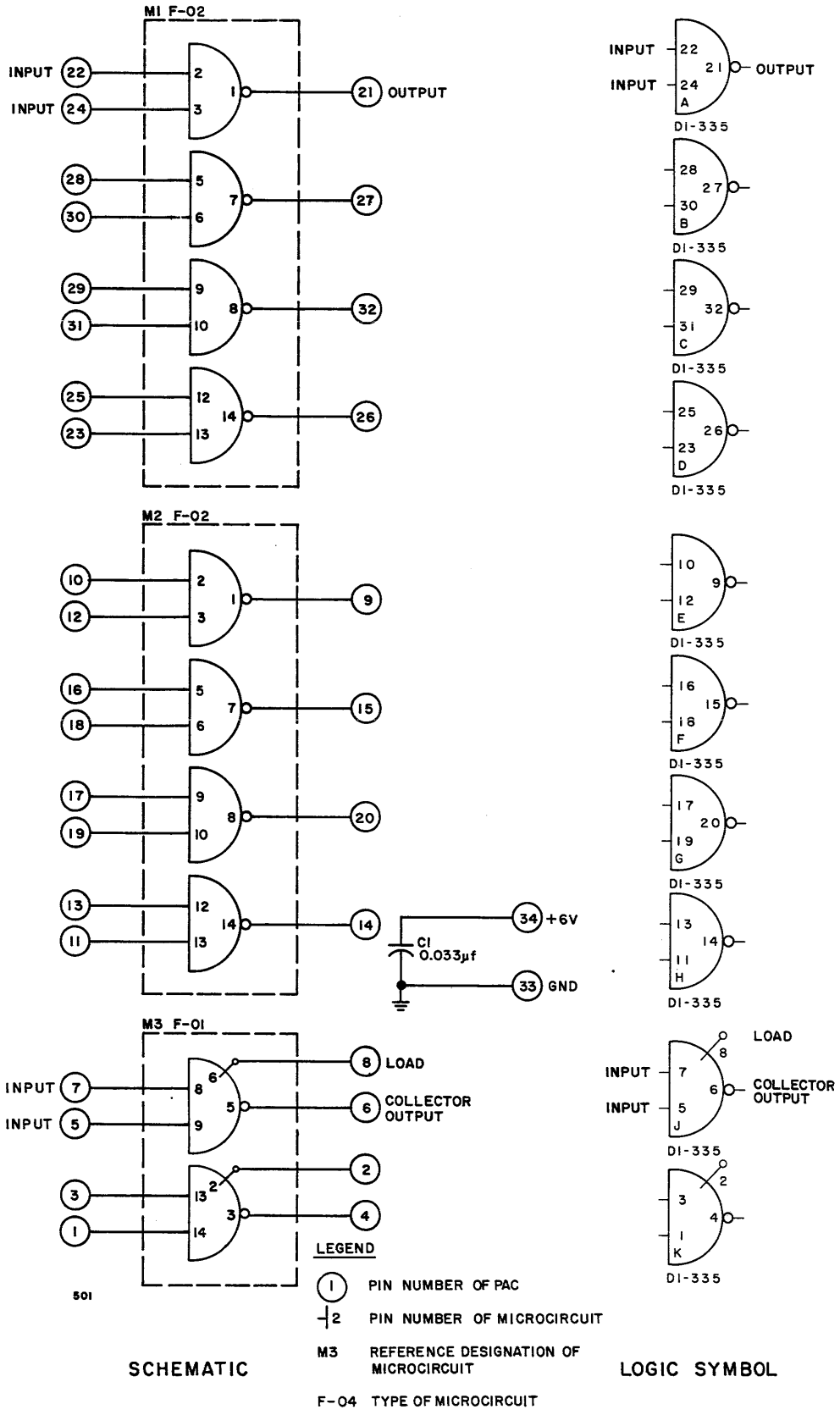


Figure DI-335-1. NAND Type 1 PAC, Schematic Diagram and Logic Symbol

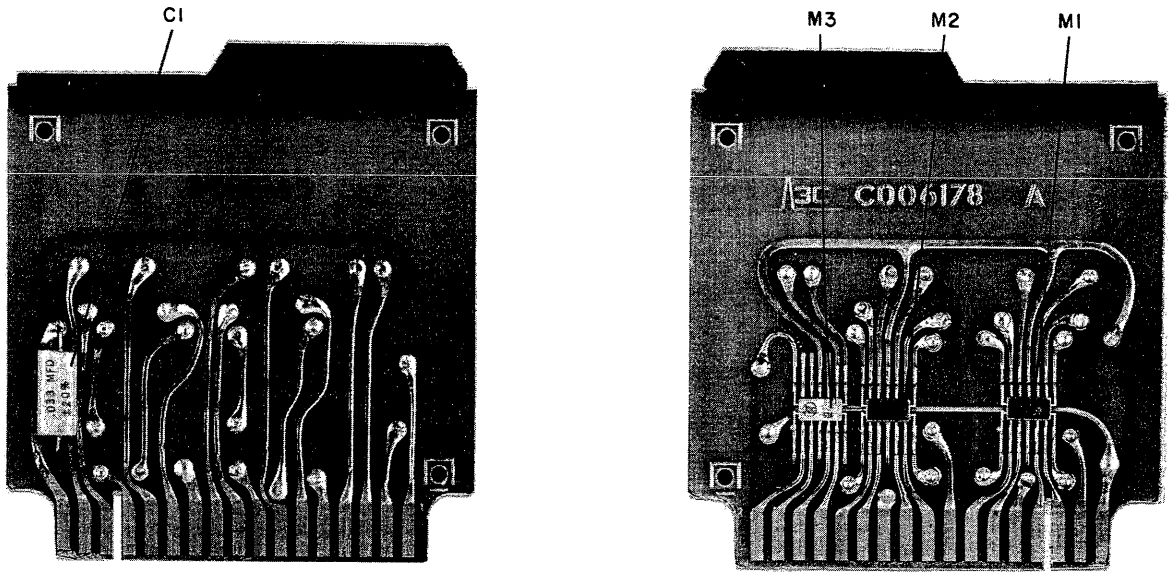


Figure DI-335-2. NAND Type 1 PAC, Parts Locations

Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1, M2	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
M3	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	930 313 016

APPLICATIONS

The NAND gates operate on levels, pulses, or combinations of both. Two gates can be wired back-to-back to form a dc set-reset flip-flop.

The two gates with separate load outputs form standard NAND gates when the load and collector output terminals are connected. When the collector outputs of gates are connected in parallel as in Figure DI-335-3, the AND-OR-INVERT function is performed. At the point where the outputs are tied together, an AND operation with logic ONEs (OR operation with logic ZEROs) takes place.

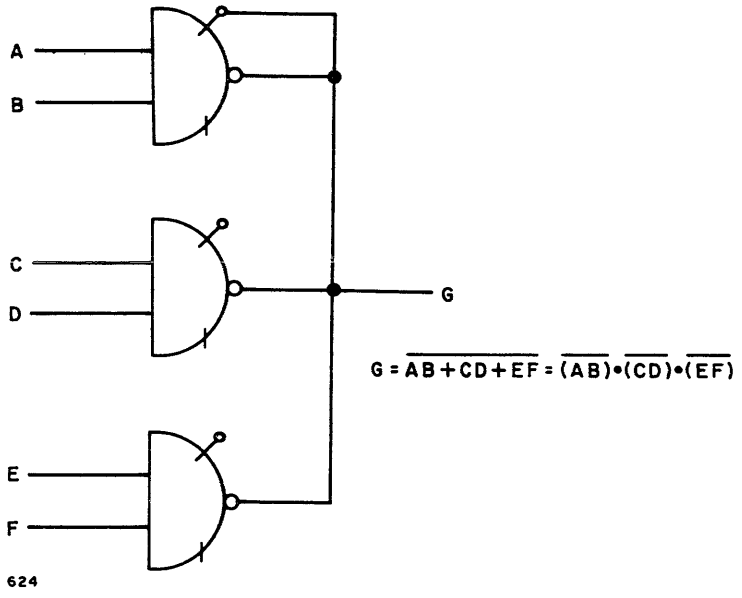


Figure DI-335-3. NAND Type I PAC, Gates Used in Parallel

EXTENDER PAC, MODEL XP-330

The Extender PAC, Model XP-330 (Figure XP-330-1), provides unobstructed access to any μ-PAC while it is electrically mounted in its appropriate μ-BLOC connector. The connector terminals at the front end of the XP-330 mount into any μ-BLOC connector and the connector at the rear accepts the μ-PAC it is displacing. Front and rear terminals are directly tied together electrically.

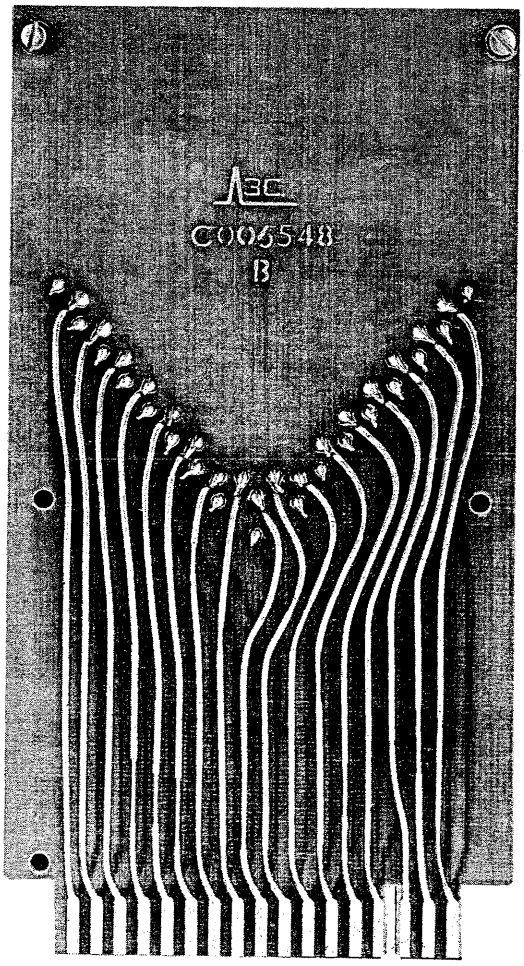


Figure XP-330-1. Extender PAC

CHAPTER III
CSM-150 CORE MEMORY MODULE

SECTION 1
INTRODUCTION

GENERAL DESCRIPTION

The 8192-word CSM-150 Core Memory Module, used for the Type 316 processor main memory, has a word length of 17 bits. The 17th bit is not used if the mainframe does not have the parity option. The nominal memory cycle time is 1600 ns. The module occupies one 1-by-3 location in the processor drawer and can be paralleled with up to three modules on a single memory bus. A 4096-word, 17-bit memory module is also available for mainframes requiring only 4096 words of memory. Expansion above 4096 or 8192 words is allowable in 8192-word increments only.

Physical Description

The core memory module is packaged on a backplane with 7 rows of 3-connector-high assemblies. The connectors are mounted on 0.375-inch centers. Each connector is 2.3 inches long and has a double row of 34 solderless-wrap pins. The backplane assembly, when mounted in the H316 drawer, takes the same area as the CSM-160 Core Memory Module but requires extra height, which is available in the drawer. The printed circuit board used in the design is the MACRO-PAC with three connector tongues. The MACRO-PAC measures 8.45 by 4.5 inches. The core plane unit is a two-board folded design that plugs into two rows of six connectors. The X and Y drive electronics is packaged on one printed circuit board, and the sense-digit electronics is packaged on two printed circuit boards, thus requiring three rows of connectors for circuit boards. The I/O and module-to-module interconnections are accomplished by using cable PACs that plug into two connectors in each outside row of the backplane assembly.

Electrical Design

The CSM-150 Core Memory Module is built around a magnetic core array wired in a 3D, 3-wire organization, where each core is threaded by three wires; two of these wires are used for addressing a word, and the third is used for both reading and writing data in the bits of a word. Integrated circuits are used for addressing and read sensing, and a transformer-coupled discrete transistor driver is used for writing. The remaining circuits

are of the common or high-speed TTL type, with open-collector drivers on all outputs. The required memory voltages are +6, -6, and +15 Vdc, with the last one requiring temperature compensation for operation over the specified temperature range. The data outputs from the module are the outputs of open collector hex buffers.

SPECIFICATIONS

General

Organization	3-wire, 3-D coincident current
Capacity	4096 or 8192 words, expandable in 8192-word increments only
Word Size	17 bits
Addressing	Random access
Modes of Operation	Clear-Write Read-Write
Cycle Time	1600 ns (maximum rate at which memory may be cycled for all modes)
Access Time	350 ns max from MXYTM+ input

Physical (Nominal)

Width	2-3/4 in. (7.00 cm)
Length	9-7/16 in. (24.00 cm)
Thickness	5-3/4 in. (14.60 cm)
Weight	2.3 lb (1.05 kgm)

Environment

Operating Temperature	0 to +60°C
Storage Temperature	-55 to +85°C
Relative Humidity	95% without condensation
Cooling	220 linear ft per min.
Altitude	15,000 ft max.
Magnetic Fields	3.0 gauss max. magnetic field strength at the core plane

Power

Current requirements are listed in Table 3-1-1. The +6 Vdc and -6 Vdc inputs must be held within ±5 percent at the backplane of the core memory module. The +15 Vdc must be within the range shown in Table 3-1-2 at the backplane pins. Current drain on the

+15 Vdc supply and power dissipation in the core memory module are strongly dependent on the number of data zeros being written into the memory.

Table 3-1-1.
Current Requirements

Voltage, Vdc	Current, Amperes	
	Active	Standby
+6	1.27	1.01
-6	0.25	0.25
+15	3.50	0.32

Table 3-1-2.
Operating Limits of Temperature-Compensated 15 VDC Supply

Temperature, °C	Limit, Vdc
0	15.6 ± 0.6
25	15.0 ± 0.8
60	14.0 ± 0.6

Interface

Input, Standard	One standard TTL load -2.0 mA max. at +0.4V +50 μA max. at +2.4V +1.0 mA max. at +5.5V Input uncertainty range, +0.8 to +2.0V
Input, Exceptions	
MXYTM+	Three standard loads
WRITE-,	Two standard loads
MADCL-A, Address and Bank Select	
Output, Standard	One open-collector drive +0.4V max. at +20 mA +250 μA max. at +5.5V All outputs are 7407 except EPARB+ (74H04) and PAMEO- (7405)

Data Retention

Data stored in the memory will not be altered during power on/off sequencing if the following conditions are met.

a. Sequencing Up -- No commands to the memory module should be initiated until all the supply voltages have attained their nominal values (within the limits of the specified tolerances). The +6 and -6 voltages should attain 90 percent of their nominal values prior to sequencing up the +15V supply.

b. Sequencing Down -- Memory cycle should not be in progress (all commands to the memory are halted) prior to or during the power down sequencing. The +15V should reach +3V prior to sequencing down the -6V and +6V supplies.

Parity

All core memory modules contain storage for the parity (17th) bit, the data register, and the parity generation electronics. These circuits are not used if the CPU does not have the parity option.

SECTION 2
OPERATING PROCEDURES

OPERATING MODES

The core memory, when commanded by the processor, performs read or write cycles at 1600 ns or slower. The address, mode, and exact timing of these cycles are controlled by the processor. All operating modes, each requiring one memory cycle, are listed in Table 3-2-1.

Table 3-2-1.
Operating Modes

Mode	Description
Read-Write	One word read from storage onto memory data output bus. Storage location cleared by fetch but written into storage from data input bus.
Clear-Write	One word in storage cleared and written with new data from memory data input bus.

ADJUSTMENTS AND LIMITATIONS

Adjustments

No operating adjustments are required for the core memory module. The power supply voltages and strobe calibration should be checked, as specified in Section 6.

Limitations

Cooling. -- Systems containing core memory must not be operated unless the cooling system is functioning properly. Fan failures longer than 30 seconds cause overheating and may damage components. Blockage of cooling by cables or dust must be avoided to ensure cool air at a uniform temperature (±5°C) to all core memory modules operated from a single temperature-compensated power supply.

Looping. -- Higher memory reliability and lower power drain are achieved if a single cycle loop is avoided. Preferred loops occupy two or three cycles and contain mostly ONEs in instruction and operand words.

SIGNALS

The following signal descriptions assume the reader has some familiarity with the organization and operation of the core memory module. Persons unfamiliar with the module should read Section 3, Functional Theory of Operation.

Address Interface Signals

Address Inputs (MADD04+ through MADD16+). -- Input signals to the address registers are single ended and are stored in registers under the control of MADCL-A.

Bank Select Input (BANKX-). -- The memory bank-select input, a single-ended signal, is stored in a register under the control of MADCL-A. A ground level on BANKX- signifies module selection. BANKA-, BANKB-, BANKC- and BANKD- control memory modules A, B, C and D, respectively.

Data Interface Signals

Data Inputs (M01FF+ through M16FF+). -- Data inputs to the inhibit drivers are single ended and buffered through a 74H04. A high data input during the write cycle results in no inhibit current, and a ONE will be stored in the memory.

Data Outputs (MM01F- through MM16F-). -- Data outputs are single ended and supplied in open collector 7407 gates for wire-OR'ing with other modules. A negative data output pulse signifies a ONE output from the memory.

Timing and Control Interface Signals

Memory Read/Write Timing (MXYTM+). -- MXYTM+ is a single rail, positive-going double pulse that starts the read and write cycle timing in the core memory module.

Memory Strobe Enable (MSTEN-). -- MSTEN- is a single rail input to the core memory module that, when low, enables the memory sense strobe generation circuit.

Memory Address Register Clear Command (MADCL-A). -- Address register clear command is a single rail negative pulse whose trailing edge latches the address and bank register flip-flops. It is also used as parity data register clear pulse.

Write Enable (WRITE-). -- Write enable, a single rail negative pulse, gates the MXYTM+ command to generate the write timing for the core memory module.

Parity Bit Data Output (PAMEO-). -- The sense data output of the parity bit is stored in the parity data register, and the buffered output of the register (PAMEO-) is transmitted to the processor for parity error checking.

Parity Generator Output (PAGEO-). -- This is the output of the parity tree transmitted on a single rail to the processor.

Parity Error Strobe (EPARB+). -- This is a parity strobe pulse generated in the core memory module and transmitted single rail to the processor for parity error strobing.

SECTION 3
FUNCTIONAL THEORY OF OPERATION

BASIC OPERATION

The core memory module consists of an array of 139,264 ferrite cores including those for the parity bits, surrounded by interface and control electronics. The core plane serves as a storage device due to the magnetic properties of the ferrite cores. Each ferrite core has two possible stable magnetic states, arbitrarily called ONE and ZERO. The act of writing a ONE consists of altering or switching a ferrite core from its ZERO state. To write a ZERO, the ferrite core is prevented or inhibited from altering its state. To read a ONE, the ferrite core is switched from its ONE to its ZERO state. The change of flux thus produced develops a voltage that is detected by the sense amplifier connected to the sense-inhibit line. To read a ZERO, the core remains in its ZERO state; therefore, no change of flux is detected. The purpose of the electronics surrounding the core array is to detect a particular word-set of cores in the array and either clear them and write in new data, or sense them and then, since the word has been set to ZERO in order to sense it, save and rewrite the sensed data back into the word. The time taken by either of these two operations, clear-write or read-regenerate, is one memory cycle.

FUNCTIONAL ELEMENTS

LBD 8114, Drawing No. 70032889, in Section 9 best illustrates the CSM-150 Core Memory Module. For additional details of each functional element and circuit, see Section 4, Detailed Theory of Operation, and the logic block diagrams in Section 9.

Storage Array

The storage array, which is the core plane, consists of 139,264 ferrite cores, including the parity bit, wired into an array to permit access of one of 8192 words (17 bits per word) per memory cycle. Addressing the array requires selecting one of the 128 X-lines and one of the 64 Y-lines and pulsing these lines with two address selection currents (nominally 400 mA in amplitude and 300 ns wide) twice per cycle. The core plane is also threaded with 17 sense-inhibit lines, each passing through one ferrite core at each of the 8192 different X- and Y-line intersections. In every cycle each sense-inhibit line requires a nominal 750 mA, 350 ns wide inhibit current, if, in that bit, a ZERO is to be written. A data output from the array on the sense-inhibit winding is a differentially sensed voltage, approximately 38 mV for a ONE and less than 12 mV for a ZERO. Included on the core plane are 8-by-8 and 8-by-16 bipolar diode matrices which, coupled with the inherent 64-by-128 decoding in the array, simplify the addressing of 8192 separate words. These diodes are packaged in a 14-pin dual in-line package with 16 diodes per package. In the

two-diodes-per-line selection scheme used in this design, 16 DIPs (256 diodes) for the X-line selection (128 lines) and 8 DIPs (128 diodes) for the Y-line selection (64 lines) are required, thus making a total of 24 diode DIPs to complete the X-line and Y-line selection for the 8192-word core plane.

Selection Interface Circuits

Address selection currents are driven through the storage array from selection interface circuits, via the X- and Y-diode matrices. The address bits (13 for an 8192-word memory and 12 for a 4096-word memory) and Bank-Select signal supplied to the memory are latched in registers within the core memory module. These registers are set up before a memory cycle and remain stable for the duration of that cycle. The MA04 address register output is disabled for 4096-word memories, as shown in LBD 8101, Drawing No. C70032890, in Section 9. Selection circuits decode the address bits to select and drive a unique word in the memory. All currents are disabled if the core memory module is not selected by the BANKX- signal.

Write or Regenerate Interface Circuits

The core memory module contains 17 write circuits, one per bit in the data word. The information present on the data input bus lines is used to write data into the memory. During the second, or write, portion of a memory cycle, a write-inhibit current will be supplied to the core array if that data bit is to be stored as a ZERO. No inhibit current occurs if a ONE is to be written. Write circuits are required to write data in a word being read (Read-Write cycle) as well as to alter the stored data (Clear-Write cycle).

Read Interface Circuits

The core memory module contains 17 read circuits, one per bit in the data word. During the first, or read, portion of a memory cycle, the sense amplifiers, at strobe time, discriminate between the core ONE and ZERO signals on the sense-inhibit lines. If a ONE is detected, the Memory Data output bus is pulled to ground for the time shown in Section 9, LBD 8110, Drawing No. C70032895. If a ONE is not detected in a bit, no action occurs, and the data output bus remains high.

Timing and Control Circuits

Input signals MXYTM+ and WRITE- control the majority of timing in the core memory module. These signals are gated and buffered to control the inhibit-current pulse widths and delayed to provide the proper read- and write-drive current timings.

The sense amplifier strobe pulse is generated by a one-shot during the read portion of a read-write cycle. The MSTEN- input gates the sense amplifier strobe during a read-write cycle.

Parity Logic

Electronics to generate odd parity during every memory cycle are included in every core memory module. Also included is a parity data register to store the parity bit data output from the read portion of a read-write cycle for use later in the cycle for parity error check and parity rewrite.

The output of the parity generator is buffered through two separate buffers to drive two individual memory interface lines, PAGEO- and PAMEO-. The signal PAGEO- indicates to the processor the output state of the parity generator for comparison with PAMEO-.

The buffered outputs of the parity register and parity generator output (gated with LPREG+) are collector-OR'ed to drive the memory interface line PAMEO- and also tied internally to the memory write interface circuits to close the parity regeneration loop.

The use of parity by the processor is an optional feature at the CPU.

SECTION 4
DETAILED THEORY OF OPERATION

STORAGE ELEMENT

Information in a core memory is stored in an array of ferrite toroidal cores. Each core may be individually set to one of two magnetic states, thereby representing one bit of binary information. A discussion of ferrite core storage is best conducted in terms of the core B-H relationship, shown in Figure 3-4-1. Magnetizing force, H, is proportional to the total current on wires passing through the core. Magnetic flux density, B, is proportional to the resulting magnetization of the core. Figure 3-4-1 illustrates two useful properties of the core. First, the core is a threshold element. A core in state B_0 remains in that state if a magnetizing force of magnitude H_1 or less is applied and removed. Second, the core is a memory element. If a larger magnetizing force, H_2, is applied, the core switches from the state of negative magnetic flux density, B_0, to the state of positive magnetic flux density, B_1, and remains there even after H is reduced to zero. The core remains in state B_1 until an equally strong magnetizing force in the opposite direction switches it back to B_0. Figure 3-4-1 also illustrates one difficulty of core storage. In order to sense the state of a core it is necessary to measure the change in B resulting from the application of a force H, and the change in B is almost undetectable until that force exceeds H_1. Therefore, a core must be switched to be sensed.

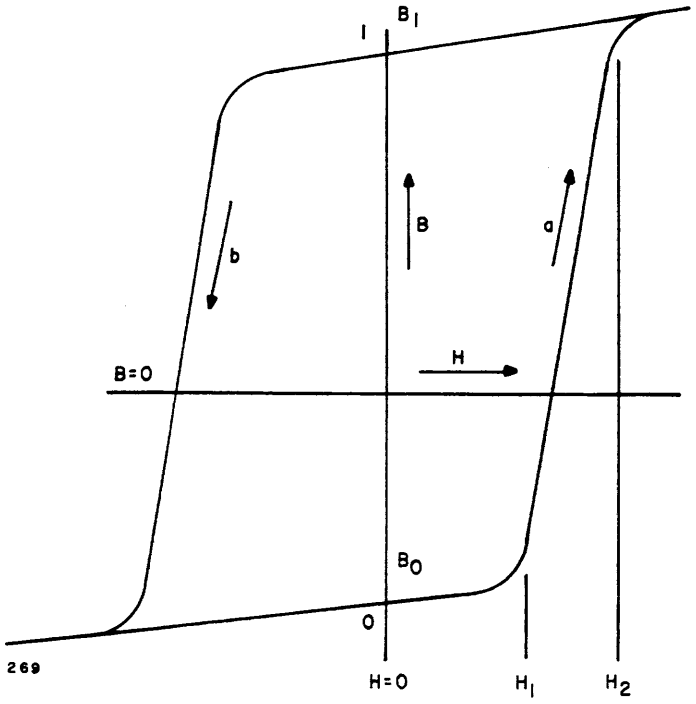
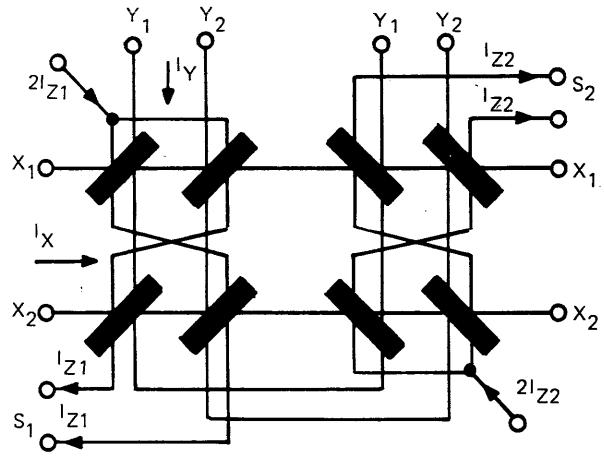


Figure 3-4-1. Ferrite Core B-H Characteristics

Read-Write Cycle and Coincident Current Selection

The storage array is formed by arranging cores and wiring so that there are as many sets of cores as there are bits in the storage word. In each set of cores a common sense-inhibit wire threads every core, and running through all sets are X- and Y-address selection lines that intersect each other only once in each bit-set of cores. A two-bit, four-word array is shown in Figure 3-4-2.



	I_X	I_Y	I_Z
READ HALF CYCLE	$+1/2\ I_F$	$+1/2\ I_F$	0
WRITE HALF CYCLE ONE	$-1/2\ I_F$	$-1/2\ I_F$	0
WRITE HALF CYCLE ZERO			$+1/2\ I_F$

$1/2\ I_F < I_T < I_F$

WHERE I_T IS THE MINIMUM CURRENT REQUIRED TO SWITCH A CORE.

Figure 3-4-2. Two-Bit, 4-Word, 3D, 3-Wire Core Array

Figure 3-4-2 shows that if a current, slightly weaker than required to switch a core, is applied to one X-line and one Y-line, then only one core per bit mat will see a current $I_x + I_y$ strong enough to cause switching. If that core switches, a voltage is induced in the sense winding for that bit and shows up at the sense terminals, S_1 or S_2. A core that switches as a result of such read-select currents is defined as having been in the ONE state. All cores in the selected word are then in the ZERO state after the read-select currents have ended, either because they were already ZERO, or because the read currents switched them to ZERO. After the read half cycle currents have read and cleared the word, write half cycle currents are applied to the same X- and Y-lines. These currents are equal to, but of opposite polarity from, the read-select currents. Again, only one core per bit set may see a total current strong enough to cause switching. The write half cycle currents drive all the bits in the selected word back to the ONE state. If a ZERO is to be written into a particular bit instead of a ONE, the sense-inhibit winding for that bit is driven with an inhibit current $2I_{Z1}$, which cancels one write-select current in the selected core. The inhibit current prevents that core from switching out of the ZERO state. As many inhibit currents are required as there are ZEROs in the word to be written. Study of Figure 3-4-2 will prove that the inhibit current does not add to any write select currents, so no other core in that bit-set will be switched during a write half cycle.

Figure 3-4-3 shows the means of connecting two diodes to one end of each X- or Y-selection line and bussing the other ends of the selection lines to form a 2-by-2 bipolar diode matrix. The matrix permits driving a particular selection line, without driving any other line, by selection of one bus line and one pair of drive lines (one drive line for each current polarity). The simplified matrix shown is not efficient, but the actual matrix is efficient, since one of the two matrices, namely the Y-matrix on the core plane, addresses 64 drive lines with only eight bus lines and eight drive line pairs. The X-matrix addresses 128 lines with 16 bus lines and 8 drive line pairs. A 4096 word memory module has an 8192 word core plane, but half the X address lines are disabled by the MA04 address register wiring change shown in Section 9, LBD 8101, Drawing No. C70032890.

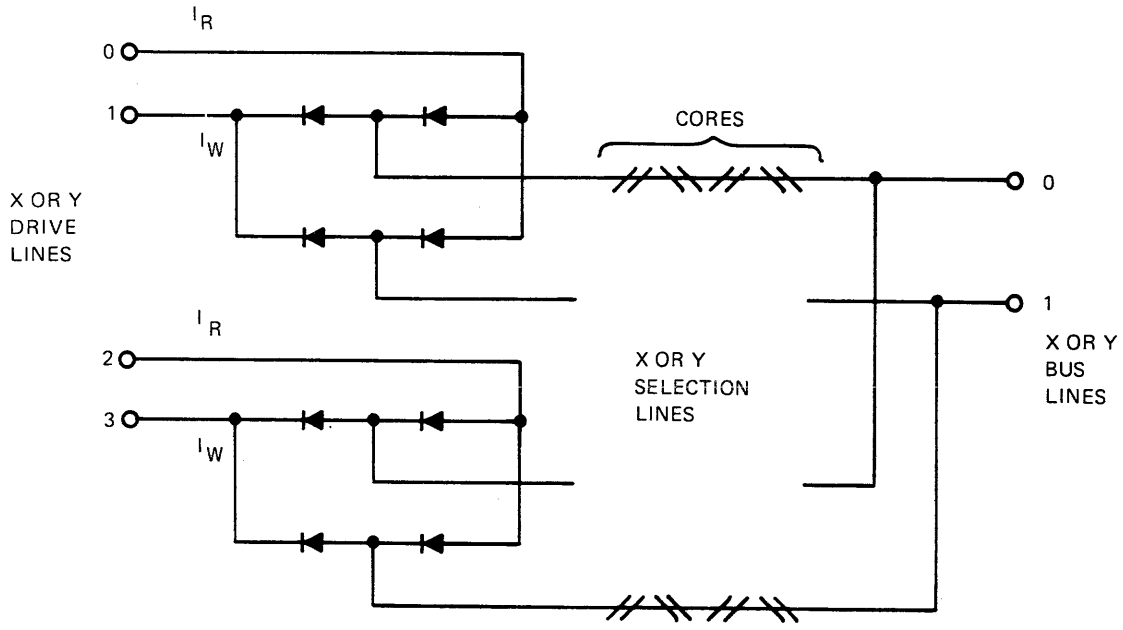


Figure 3-4-3. Two-by-Two Bipolar Diode Matrix

SELECTION CIRCUITS

Selection Switches

Figure 3-4-4 illustrates how bipolar selection currents are driven through the storage array. Each switch circuit acts as a single-pole, double-throw switch. If all six address bits are true, a pair of read-timing or write-timing commands cause a current path to be completed through the selection line, from the drive current node to ground. The current flows through the selection line in either of two opposite directions, depending whether read or write timing is commanded. The core memory module contains 8 drive line switches and 8 bus line switches for the Y-axis and 8 drive line switches and 16 bus line switches for the X-axis.

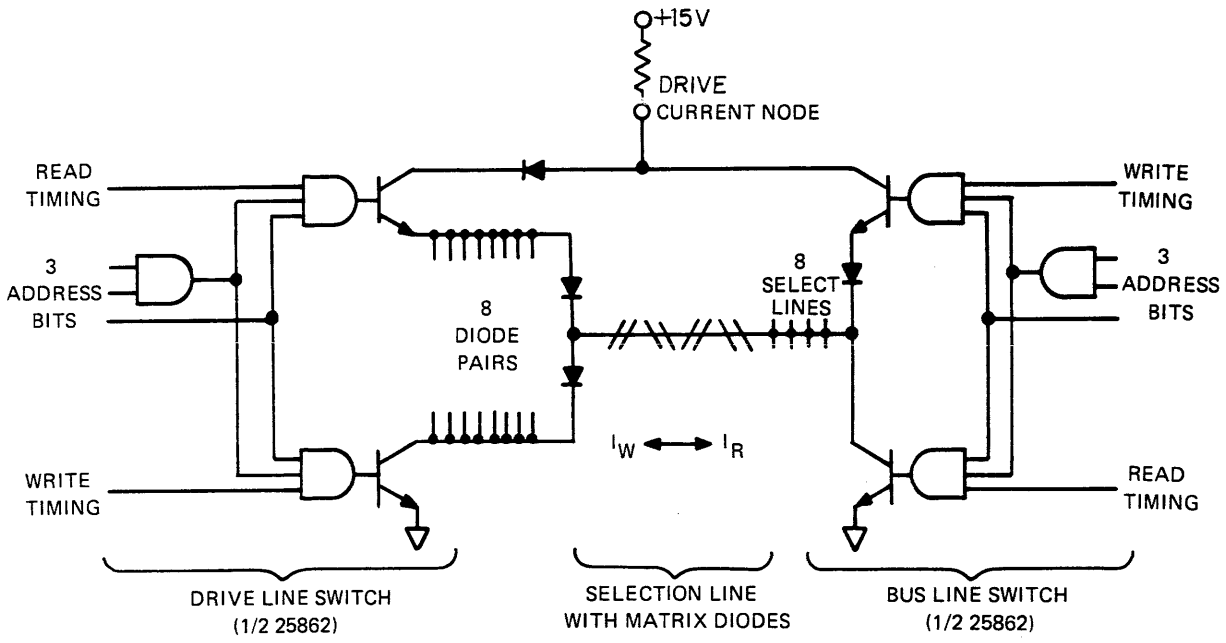


Figure 3-4-4. Selection Switches

DATA LOOP

Read Data Path

The read data path is illustrated in Figure 3-4-5. The ONE signal from the core plane is a differential signal of typically 38 mV peak amplitude, of either polarity (hence the sense amplifier exclusive-OR symbol). The ZERO signal is ideally zero, but various effects bring it up to about 10 mV at strobe time. The sense amplifier is biased with external resistors to discriminate between ONEs and ZEROs at a nominal threshold of 18 mV. The sense amplifier is strobed early in a memory cycle when the address selection noise on the sense-inhibit lines has decayed below the threshold level. If a ONE is detected, a negative going pulse appears on the data output bus. If a ZERO is present, the data output remains high. A pulse stretcher circuit on each data output circuit guarantees the minimum pulse width needed to set the memory information register in the CPU. All data output lines are from open collector 7407 buffers.

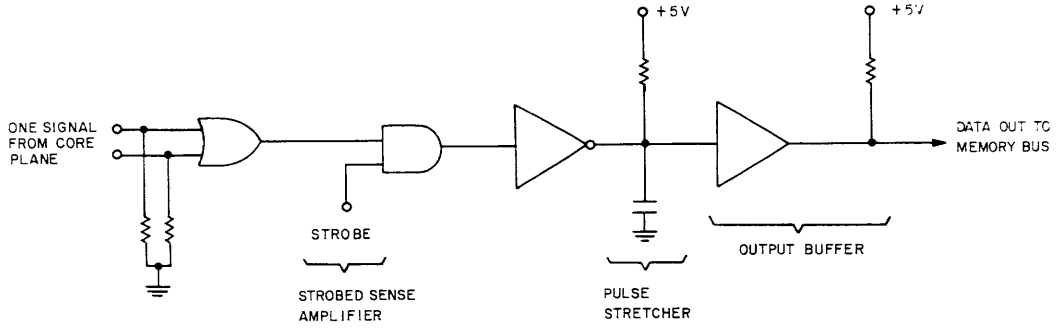


Figure 3-4-5. Read Data Circuits

There are 17 read circuits in a core memory module, including the parity bit. The 17th bit is not used if the CPU does not have the parity option.

Write Data Path

The write data path is shown in Figure 3-4-6. Inhibit current is driven into a sense-inhibit winding only when a ZERO is to be written in that bit of the word. The two-input gate turns on (ground output) at inhibit time if the memory data input is low. Current in the gate output is coupled through a 1 to 1 transformer to turn on the inhibit driver transistor. The saturated transistor completes the inhibit current path, from +15 Vdc through the sense-inhibit winding to ground. The value of inhibit current is set by the +15 Vdc supply and the inhibit resistor. A balun-connected transformer forces equal current sharing in the two legs of the winding.

When inhibit time ends and the transistor is turned off, inductance of the inhibit winding tends to continue the current flow in the same direction as before, and the inhibit driver end of that winding swings sharply to a negative voltage. The turnoff diode clamps this swing and provides a path for the current to decay exponentially to zero. There are 17 inhibit circuits in a core memory module.

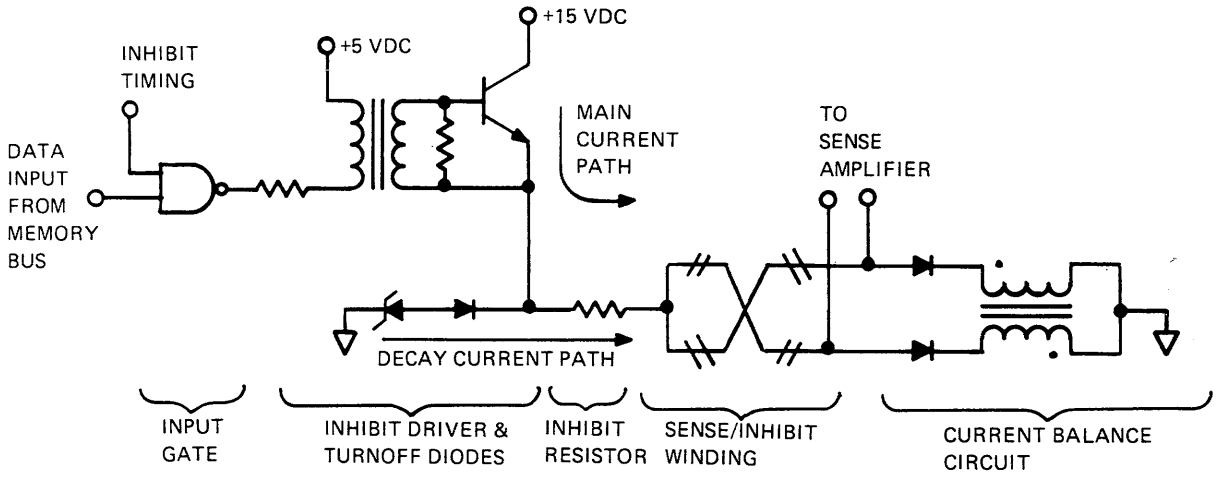


Figure 3-4-6. Inhibit Circuit

TIMING AND CONTROL

Refer to Section 9 for detailed diagrams of the timing circuits. Signal names used below follow the same conventions used in the LBDs in Section 9; that is, when several similar signals (e.g., data inputs) are described together, their differentiating characters (e.g., M01FF+) are replaced with double letters (MXXFF+). Also, signals that differ only by a suffix (INHEN+A and INHEN+B) have identical timing except for differences in gate delays.

Address and Current Timing

Prior to a memory cycle, address and bank-select are gated into registers by MADCL-A. Register outputs follow the inputs as long as MADCL-A is low.

The cycle begins with the leading edge of the first positive pulse of MXYTM+. The leading and trailing edges of this first pulse are shifted in an RLC network and combined in gates to form read current timing commands (XRSW+, XRSK+A, XRSK+B, YRSW+ and YRSK+). The second positive pulse of MXYTM+ is similarly shaped to produce the write-timing (XWSW+A, XWSW+B, XWSK+, YWSW+, YWSK+) and inhibit-timing (INHEN+A and INHEN+B) signals.

Data Loop Timing

Sense amplifier strobe (STROB-) timing is generated by ANDing three signals: XRSW+ (read current timing signal), MSTRB- (reset output of a one-shot triggered from YRSK+), and MSTEN+ (buffered memory strobe enable input from the CPU).

The XRSW+ input removes a race condition due to triggering delay in the one-shot and also defines the trailing edge of strobe. The MSTRB- input defines a critical timing edge, the leading edge of strobe. The MSTEN+ input disables the strobe pulse during clear-write cycles. The strobe pulse enables the sense amplifier data to the data output bus through the pulse stretcher and buffer.

Parity Logic

The electronics and logic associated with the parity bit consist of the following:

a. The 17th bit (parity bit) read data path,
b. The 17th bit (parity bit) write data path,
c. The parity generator,
d. The parity data register.

The 17th bit, read-data and write-data paths have previously been explained. The parity generator consists of two 8-bit parity generator checker circuits (PG1 and PG2) connected in series to generate odd parity. The system data input lines are broken into two 8-bit groups. The buffered outputs of M01FF+ through M08FF+ drive PG1, and the output of PG1 and buffered outputs of M09FF+ through M16FF+ drive PG2 (see Figure 3-4-7). The output of the parity generator is buffered through the 7404 and 7407 gates to drive the memory interface line designated PAGEO-. The output of PG2 is also gated with a timing pulse called LPREG+. The output of this gate is collector-OR'ed with the parity register's buffered output to control the interface signal line called PAMEO-. The PAMEO- has two functions depending upon the memory cycle in progress. During a read-write cycle the 17th bit is stored in the parity register and PAMEO- is used to compare with PAGEO- at the processor end. It is also tied internally to the write interface to complete the regeneration or write portion of the cycle. During clear-write cycles PAMEO- is controlled by the gated output of PG2 to write the parity information into the memory.

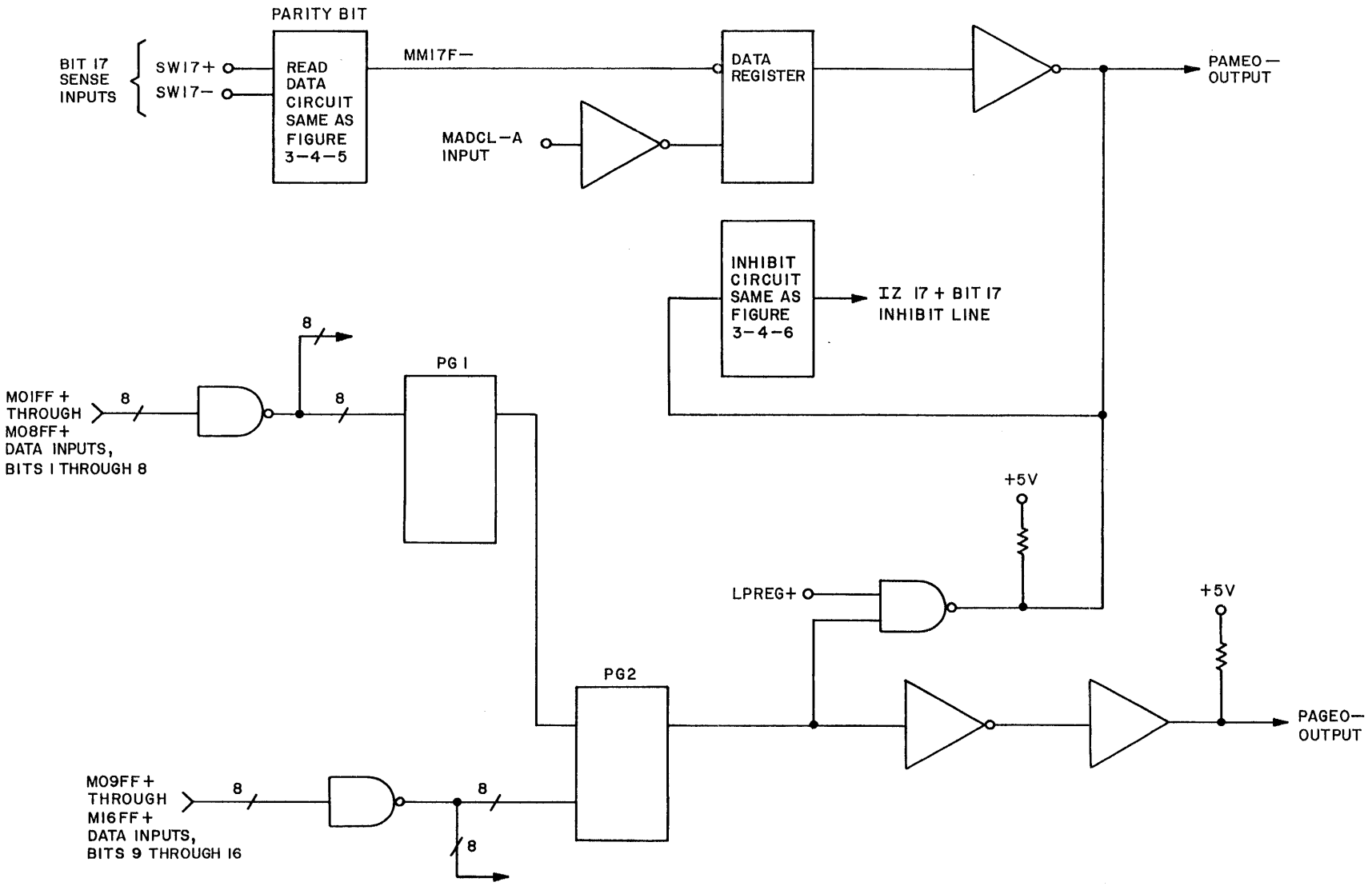


Figure 3-4-7. Parity Generation and Register Logic

TIMING DIAGRAMS

Refer to Section 9, LBDs 8110 and 8111, Drawing No. C70032895 and C70032897, for interface and internal timing, respectively.

SECTION 5
INSTALLATION

Service personnel should be familiar with the complete installation procedure and the interface requirements before attempting to install the core memory module.

TOOLS AND TEST EQUIPMENT

Table 3-5-1 lists the tools and equipment required to install the core memory module.

Table 3-5-1.
Installation Tools and Test Equipment

Quantity	Description	Type or Equivalent
1	Digital voltmeter	Honeywell Model 623 (±0.05% F.S., 1 Megohm Input Resistance)
1	Trimpot adjustment tool or screwdriver	
1	Screwdriver	Phillips
2	Screw, pan head	70904113021
2	Lockwasher, split	70902006078
2	Washer, flat	70902054003
2	Bushing, insulated	70916300007
2	Spacer	A700322753701

SPACE AND ENVIRONMENT

The core memory module occupies the same space as a 1-by-3 omni-BLOC. Environmental specifications are listed in Section 1.

INTERFACE CONSIDERATIONS

The interface requirements are met by inserting the two I/O cable PACs into the appropriate connector slots provided in the memory connector block. Interface pin connections and cable PAC locations are shown in LBD 8112, Drawing No. C70032896, in Section 9.

INSTALLATION PROCEDURES

Unpacking, Repacking and Reshipping

Upon receipt of the core memory module, care must be exercised in unpacking. A thorough visual inspection should be made for damage and loose hardware. Check for

foreign objects between the core plane boards. Extreme caution must be observed to prevent any object from penetrating into the core plane area.

Should reshipping become necessary, wrap the module in plastic, seal with tape, and place in a sturdy cardboard box with more than one inch of resilient packaging on all sides.

Mechanical Procedures

Insert the core memory module with the circuit boards side up in the upper level of the chassis. Use the spacer, tools, and mounting hardware outlined in Table 3-5-1.

Electrical Checkout Procedure

To perform the electrical checkout procedure,

a. Load the Core Memory Test Program, CMT5, Document No. 70181454000.

b. Run the diagnostic test in the installed module.

c. Halt the program, fetch any location in the module, turn power off and on, and fetch the location again to see that it is unchanged.

d. Perform the voltage and strobe margin checks described in Section 6.

SECTION 6
MAINTENANCE

EQUIPMENT CONFIGURATION

Mechanical Assemblies

The mechanical components of the core memory module are shown in Section 10. There are five major subassemblies: three circuit boards, one core plane, and one solderless-wrap connector backplane.

Module Location

The core memory module occupies the same area as a 1-by-3 omni-BLOC. Since the CSM-150 Core Memory Module is higher than a CSM-160 Core Memory Module, it requires slightly different mounting methods, as described in Section 5.

OPERATOR MAINTENANCE

No operator maintenance is necessary on the core memory module. The operator should periodically check the cooling fans and air filters.

STANDARD MAINTENANCE

Tools and Test Equipment

The tools and equipment listed in Table 3-6-1 are needed for maintenance and troubleshooting in addition to those listed in Table 3-5-1.

Table 3-6-1.
Troubleshooting and Maintenance Tools and Test Equipment

Quantity	Description	Type or Equivalent
1	Oscilloscope	Tektronix 454
1	Multimeter	Simpson 260
3	Card Extender PACs	Honeywell XP-330
1	MACRO-PAC Extractor Tool	Honeywell B70026032701
1	AC Current Probe	Tektronix P6020
1	Hand Wire-Unwrapping Tool	Gardner-Denver 505244
1	Hand Wire-Wrapping Tool, Battery-Operated	Honeywell 70917200001 (Gardner-Denver No. 14R2)
1	Wire Stripper	Honeywell 70917250001 (Ideal 45-179)

Table 3-6-1. (Cont)

Quantity	Description	Type or Equivalent
5 Ft	No. 30 AWG Solid Wire	Honeywell 70940061010
1	Quick Disconnect Terminal Crimper	T & B WT 145

Preventive Maintenance

Cleanness. -- The core memory module must be kept free of dust, dirt, and any foreign objects. The air filter of the cooling system must be kept clean to ensure sufficient air flow. Should it be necessary to clean the core plane, only use de-ionized water. However, cleaning the core plane is not recommended as a field procedure.

CAUTION

Never use an air hose to clean the core plane.

Margin Checks. -- The power-supply margin checks can detect performance degradation before operational failures occur. The memory drive and inhibit currents are determined by the setting of the +15 Vdc supply and the resistors on the CM-866 and CM-867 boards. The +15V supply setting should be periodically checked by using a voltmeter capable of reading the voltage within ±1 percent. Measurements should be made at the memory terminals while a program is running in the memory. The CMT5 diagnostic program contains several test patterns, including the worst pattern (exclusive-OR of MAD13- and MAD08-), all ONEs and all ZEROs. Failure points at the high +15V setting (do not exceed +17.5V) and low +15V setting should be noted; their differences should be at least 1.6V at 25°C and 1.2V at 0 and 60°C. The +15V supply should be set at the center of the failure point margins. Temperature tracking specifications are listed in Section 1.

Adjustment

The core memory module has no adjustable components. The timing of the sense amplifier strobe pulse is set at Honeywell Inc. for each unit to give optimum operating margins. It is not necessary to adjust the strobe timing. If a change in timing is required to obtain proper memory operation, the associated boards and core plane should be checked before a change is made.

Table 3-6-2 presents the strobe jumpers that can be added for test purposes to uncover marginal operation. The jumper locations are shown in Figure 3-10-1 in Section 10 and on LBD 8101, Drawing No. C70032890, in Section 9.

Table 3-6-2.
Memory Strobe Test Modes

Mode	Mean	Function
Early Strobe	Jumper J_2 (between SST5 and SST2)	Increase tendency for memory to pick ONEs (detect marginal ZERO bits)
Late Strobe	Jumper J_3 (between SST1 and SST4)	Increase tendency for memory to drop ONEs (detect marginal ONEs)
Normal	No Jumpers	Normal

Removal and Replacement

The board connectors are polarized to protect against incorrect board insertion. Board removal from the memory is accomplished by engaging the cut-out in the handle of the board with the board extractor tool. Do not remove or insert printed circuit cards without turning off the dc power. Additional care should be taken when removing the CM-867 data board adjacent to the I/O cable slot in the first memory module as the cable sleeving can be ruptured due to scratching by the DIP leads on the etch side of this board.

CAUTION

Remove the boards on both sides of the core plane. This allows more room for gripping the handle when removing the core plane. Do not use the MACRO-PAC Extractor Tool or any other tool; otherwise, damage to the core plane will result.

When replacing defective components, use a low-wattage soldering iron and rosin 60/40 solder. Remove excess solder from the printed circuit board. Care should be taken to avoid lifting the etch.

SECTION 7
TROUBLESHOOTING

GENERAL PROCEDURES

The following steps should be performed before repairing the module.

a. Uncover symptoms.

b. Determine type of problems.

c. Determine section at fault.

d. Locate faulty circuit.

If the module is to be forwarded for repair, troubleshooting should nonetheless be carried at least through Step b and specifics of the problem forwarded along with the module. Include the module serial number with all documentation. If the module is to be replaced, use the checkout procedure in Section 5 on the new module. The reader should be familiar with the material in previous sections of the manual before attempting repairs other than module replacement. Refer to Section 6 for maintenance tools and procedures, Section 8 for signal mnemonics, Section 10 for mechanical assemblies, parts locations, and parts lists, and Section 9 for logic diagrams and detailed timing diagrams.

SPECIFIC PROCEDURES

Module Interchangeability

Module interchangeability involves no wiring changes. Unless the problem is a marginal condition in the processor or power supply, module swapping will isolate a faulty module. Because of the above uncertainty, diagnosis should be carried beyond module swapping. All memory boards with the same designation are interchangeable. For example, a CM-867B will replace a CM-867B, CM-867A or CM-867. A CM-867 will not be interchangeable with a CM-867A or CM-867B.*

Core Memory Test Program

The core memory test (CMT) program exercises the memory in various troublesome and diagnostic patterns and prints out errors. It is useful for uncovering and determining the type of problem.

Control Panel Debugging

Control panel debugging is invaluable if the processor cannot load and run CMT, but is almost useless for intermittent or pattern-sensitive errors. A general path to try is as

*This is an example only. CM-867A and CM-867B do not exist at this time.

follows. Store ONEs throughout the module, and examine suspect locations. Repeat with ZEROs. To check if address bit circuits are operating, go to the lowest address in the module, and store ZERO in it. Set each address bit (4 through 16) to ONE, one at a time, and store the address in itself. Fetch the lowest location again, check that it is still ZERO. Store ZERO in it again. Fetch each of the other locations stored; they should be unchanged. Any errors in the words being read will point to the address bit at fault. This test is most stringent with +6 Vdc supply to the module set 5 percent low. In all above tests, fetching two or three times at the same address will check regeneration.

Waveform Checks

Waveform checks isolate a problem to a specific circuit. The majority of signals can be observed on the backplane connector pins or the board test point terminals (labelled TP on the LBDs and assembly drawings). If additional signals must be viewed, three XP-330 μ-PAC extenders can be used.

The drawings in Sections 9 and 10 can be used to determine the proper waveforms. Common circuits (e.g., data bits) can be compared to determine signal differences. Check the CM-866 drive and timing signals if failures are common to all data bits. Observe the CM-867 sense and inhibit waveforms if failures are at all locations and at some or all data bits. Probing sense amplifier inputs requires a differential oscilloscope preamplifier and should be done carefully to avoid component damage and introduction of spurious signals.

CORE PLANE TROUBLESHOOTING

Under normal operating conditions it is unlikely that troubles will occur within the core plane. However, continuity measurements of the sense-inhibit and drive windings enable maintenance personnel to check core-plane wiring. Exercise caution in taking these measurements to avoid damaging the matrix windings.

Repair should not be attempted on the core plane since it may affect vendor warranties. A defective core plane should be returned to Honeywell Inc. for repair or replacement. A report describing failure symptoms or diagnosis should be returned with it.

CAUTION

Multimeter current and voltage should be kept below 300 mA and 30V, respectively, to avoid damage to matrix windings and components.

Sense-Inhibit Windings

a. Turn off memory power. Remove the CM-867 data board associated with the sense-inhibit windings to be checked.

b. Place the ohmmeter leads across the sense winding inputs (SWXX+ and SWXX-) to the CM-867 data board, as determined from LBD 8104, Drawing No. C70032893, in Section 9 (bits 1 to 16) or from LBD 8105, Drawing No. C70032894, (parity bit 17), and check for continuity. One sense-winding links 8192 cores.

c. Resistance readings should be typically 13 ohms (across SWXX+ and SWXX-) for all sense-inhibit windings. The resistance readings for all windings should agree within ±7 percent.

d. Measure between signals IZXX+ and SWXX+ to check inhibit wiring continuity. Results should be 6.4 ohms ±7 percent. Repeat for IZXX+ to SWXX-.

Drive Windings

a. Turn off memory power. Remove the CM-866 address board. The drive winding connections to the core plane are shown in LBDs 8102 and 8103, Drawing No. C70032891 and C70032892, respectively, in Section 9 and Figures 3-10-3 and 3-10-4 in Section 10.

b. The actual drive line connections are located on the core plane printed circuit board. The selection switch outputs are isolated by a diode from each drive line so that the resistance reading between any drive bus (e.g., XDXX) and line bus (e.g., XBXX) includes a diode forward drop.

c. Measure continuity by putting one ohmmeter probe on the XDXX (or YDXX) pin and the other probe on the XBXX (or YBXX) bus. A low resistance of one forward diode drop plus a drive line resistance of approximately 8.5 ohms indicates continuity for the diode and the drive line. It may be necessary to reverse the probes to obtain the correct polarity to forward bias the selection diodes. A high impedance measurement in both directions indicates an open line or diode.

Troubleshooting Table

Memory failures are localized by loading the test pattern into the memory and by initiating a read operation at each address sequentially and then checking each readout data word for the type of failures. Generally, memory failures are operational failures, partial data word failures, or address, decoding and selection failures. An operational failure, caused by faulty timing and control circuits, occurs when commands applied to the memory have no apparent response or when there is a faulty operation at all addresses.

Partial data word failures are caused by a faulty sense amplifier, data register flip-flop (in the processor), or by data-write circuits.

Address, decoding and selection failures are caused by a faulty address register or selection circuits. The memory operation is faulty at only particular addresses.

Table 3-7-1 lists the general type of memory failure along with symptoms and probable causes.

Table 3-7-1.
Troubleshooting Memory Failures

Failure	Symptom	Probable Cause
Operational	No apparent response to commands	1. Dc voltage 2. No timing inputs (CPU failure) 3. MXYTM+, WRITE-, MADCL-A, BANK X- signals and associated logic.
	Unable to read from any address	1. +15 Vdc supply 2. MSTEN-, STROB- 3. CPU

Table 3-7-1. (Cont)

Failure	Symptom	Probable Cause
Partial Data Word	Failure of one bit (ZERO or ONE) at all addresses	1. CM-867 data board 2. CPU data register 3. Sense-inhibit winding
	Failure of one bit at particular addresses	1. CM-867 data board 2. CM-866 address board 3. Sense-inhibit winding 4. X- or Y-drive line 5. X- or Y-selection diode
	Failure of one bit at one address	1. Marginal data board (CM-867) 2. Marginal core
Address, Decoding, and Selection	All bits fail as a function of particular address bits	1. CM-866 address board 2. X- or Y-drive line 3. X- or Y-selection diode
	All bits fail at lower or upper 4096 addresses	Configuration jumper (LBD 8101) incorrect

Cable Information

LBD 8113, Drawing No. 70032899, in Section 9 shows the locations of two μ-PAC jumper cables required for each CSM-150 Core Memory Module. LBD 8112, Drawing No. 70032895, in Section 9 shows the backplane pins for all interface signals. Power (+15 Vdc, +6 Vdc, -6 Vdc and ground) is connected to the Heyco connectors on the solderless-wrap backplane.

SECTION 8
REFERENCE DATA

The signal mnemonics for the CSM-150 Core Memory Module are listed below.

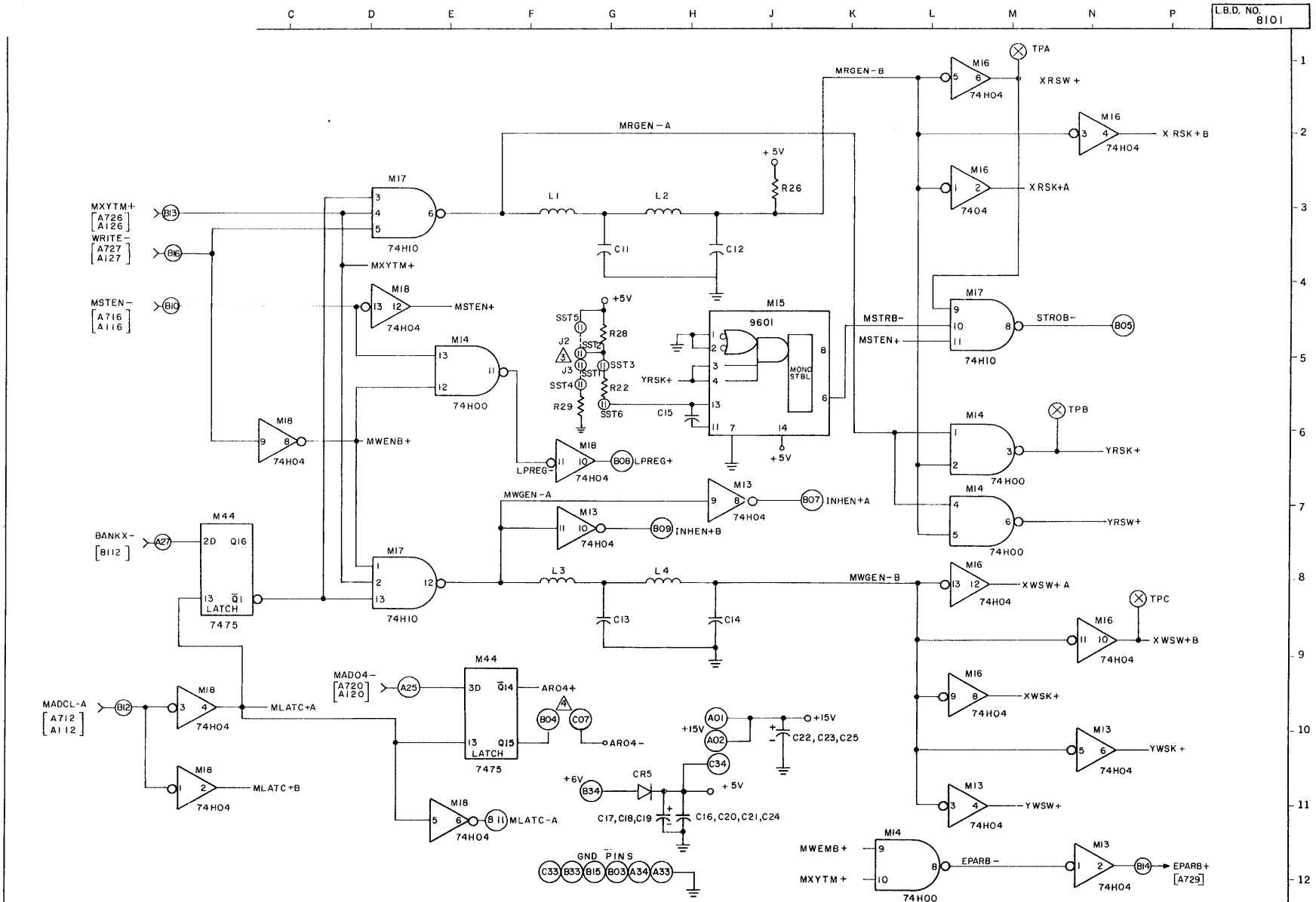
Signal	Description	LBD
BANKA- through BANKD-	Memory Bank Select Inputs	8101, 8112
INHEN+ A, B	Inhibit Timing Command	8101, 8104, 8105
M01FF+ through M16FF+	Memory Module Data Inputs	8104, 8105, 8112
MAD04- through MAD16-	Memory Address Inputs	8101, 8102, 8103, 8112
MADCL-A	Memory Address Clear Command	8101, 8112
MM01F- through MM16F-	Memory Data Outputs (sense amplifier outputs)	8104, 8105, 8112
PAMEO-	Parity Bit Data Output	8105, 8112
PAGEO-	Parity Generator Output	8105, 8112
EPARB+	Parity Error Strobe Output	8105, 8112
APGNO+	8-Bit Parity Generator Output	8105, 8112
IZ01+ through IZ17+	Inhibit Windings	8104, 8105
STROB±	Sense Amplifier Strobe Command	8101, 8104, 8105
SW01± through SW17±	Sense Windings	8104, 8105
MXYTM+	Memory Read and Write Timing Commands	8101, 8112
WRITE-	Write-Enable Timing Command	8101, 8112
MSTEN±	Memory Strobe-Enable Command	8101, 8112
MWENB+	Memory Write-Enable Command	8101
LPREG±	Load Parity Register Command	8101, 8105
MLATC+ A, B, and -A	Memory Address Latch Command	8101, 8102, 8103
AR04± through AR16±	Memory Address Latch Output Commands	8101, 8102, 8103
MSTRB-	Memory Strobe Leading Edge Timing Command	8101
MRGEN-A and MRGEN-B	Memory Read-Enable Command	8101
MWGEN-A and MWGEN-B	Memory Write-Enable Command	8101
Test Points A, B, C, and X	Test Points	8101
XRSW+	X-Read Switch Timing Command	8101, 8103
XRSK+A and XRSK+B	X-Read Sink Timing Command	8101, 8103
XWSW+A and XWSW+B	X-Write Switch Timing Command	8101, 8103
XWSK+	X-Write Sink Timing Command	8101, 8103
YRSW+	Y-Read Switch Timing Command	8101, 8102

Signal	Description	LBD
YRSK+	Y-Read Sink Timing Command	8101, 8102
YWSW+	Y-Write Switch Timing Command	8101, 8102
YWSK+	Y-Write Sink Timing Command	8101, 8102
XDCSR+	X-Diode Drive Current Source	8103
XBCSR+	X-Bus Drive Current Source	8103
YDCSR+	Y-Diode Drive Current Source	8102
YBCSR+	Y-Bus Drive Current Source	8102
SAVTH-	Sense Amplifier Threshold Voltage	8104, 8105
MIT01- through MIT17-	Memory Inhibit Bit 01 through 17	8104, 8105
M01FF-A through M17FF-A	Buffered Data Inputs	8104, 8105

SECTION 9
LOGIC BLOCK DIAGRAMS

This section includes the logic block diagrams (LBD) referenced throughout Chapter 3. The LBD number of each drawing is shown in the upper right-hand corner.

LBD No.	Drawing No.	Description
8101	C70032890	CSM-150 Memory Timing and Control, CM-866 Address Board, Slot 2
8102	C70032891	CSM-150 Memory Y-Selection, CM-866 Address Board, Slot 2
8103	C70032892	CSM-150 Memory X-Selection, CM-866 Address Board, Slot 2
8104	C70032893	CSM-150 Memory Data Bits 1 through 16, CM-867, Slots 5 and 6
8105	C70032894	CSM-150 Memory Parity, CM-867, Slots 5 and 6
8110	C70032895	CSM-150 Memory Interface Timing
8111	C70032897	CSM-150 Memory Internal Timing Diagram
8112	C70032896	CSM-150 1-by-3 Connector Wiring
8113	C70032899	CSM-150 Memory PAC Complement/ Allocation
8114	C70032889	CSM-150 Memory Block Diagram



NOTES:

4. 4K MEMORY: DELETE CONNECTION B04 TO C07; ADD B33 TO C07.
   8K MEMORY: DELETE CONNECTION B33 TO C07; ADD B04 TO C07.
3. ADD J2 JUMPER FOR EARLY STROBE MARGIN CHECK; OMIT J3 JUMPER.
   ADD J3 JUMPER FOR LATE STROBE; OMIT J2 JUMPER.
2. CM-866 SPARE GATE: M13 OUTPUT 12.
1. ○ DESIGNATES BOARD CONNECTOR AND PIN. ⟩— INDICATES CSM-150 INTERFACE SIGNAL.
   [ ] INDICATES SOURCE LBD OR I/O PIN.

REV.	REVISIONS	CHK.
A	PER ISSUE	
B	ECO 30195 EXT. CHGS PER ECO 23-1-5	
C	BLC031273 ADD DOT AT JUNCTION C34 & +5V 13-9-10	

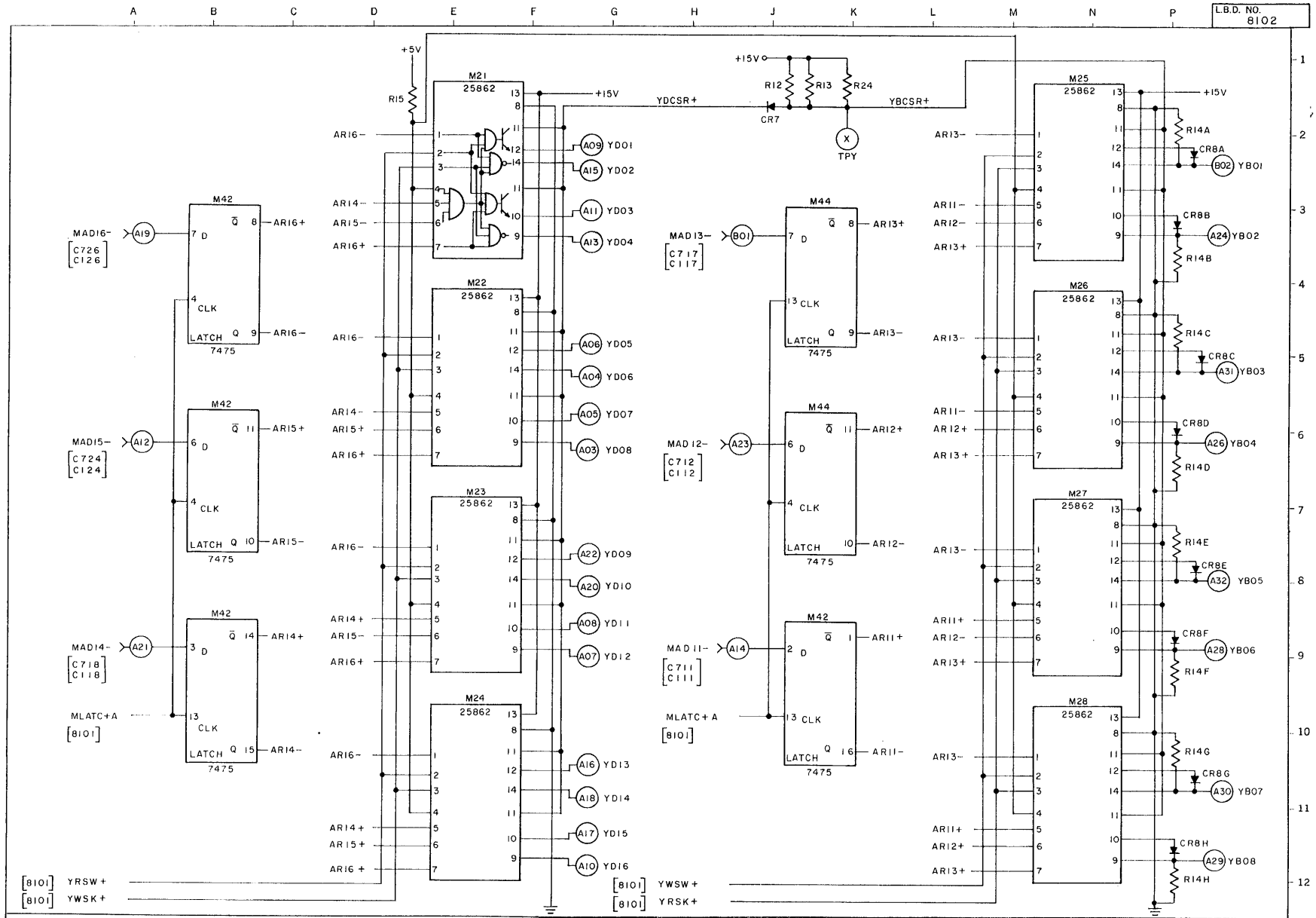
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. R. BOUDROT	DATE 8/10/72
ENG. S. DURVASULA	8/10/72
APP. D. ROTHENBERG	8/10/72
PROJECT NO. H404-01	

TITLE
CSM-150 MEMORY
TIMING & CONTROL
CM-866 ADDRESS
BOARD SLOT 2

SIZE C | DWG NO. 70 032 890 | REV. C

Form LBD F2760-571



NOTES:

1. ○ DESIGNATES BOARD CONNECTOR AND PIN. ⟩— INDICATES CSM-150 INTERFACE SIGNAL.
   [ ] INDICATES SOURCE LBD OR I/O PIN.

REVISIONS	REV.	CHK.
PER ISSUE	A	
ECO 30795 EXT. CHGS PER ECO 73-7-5	B	

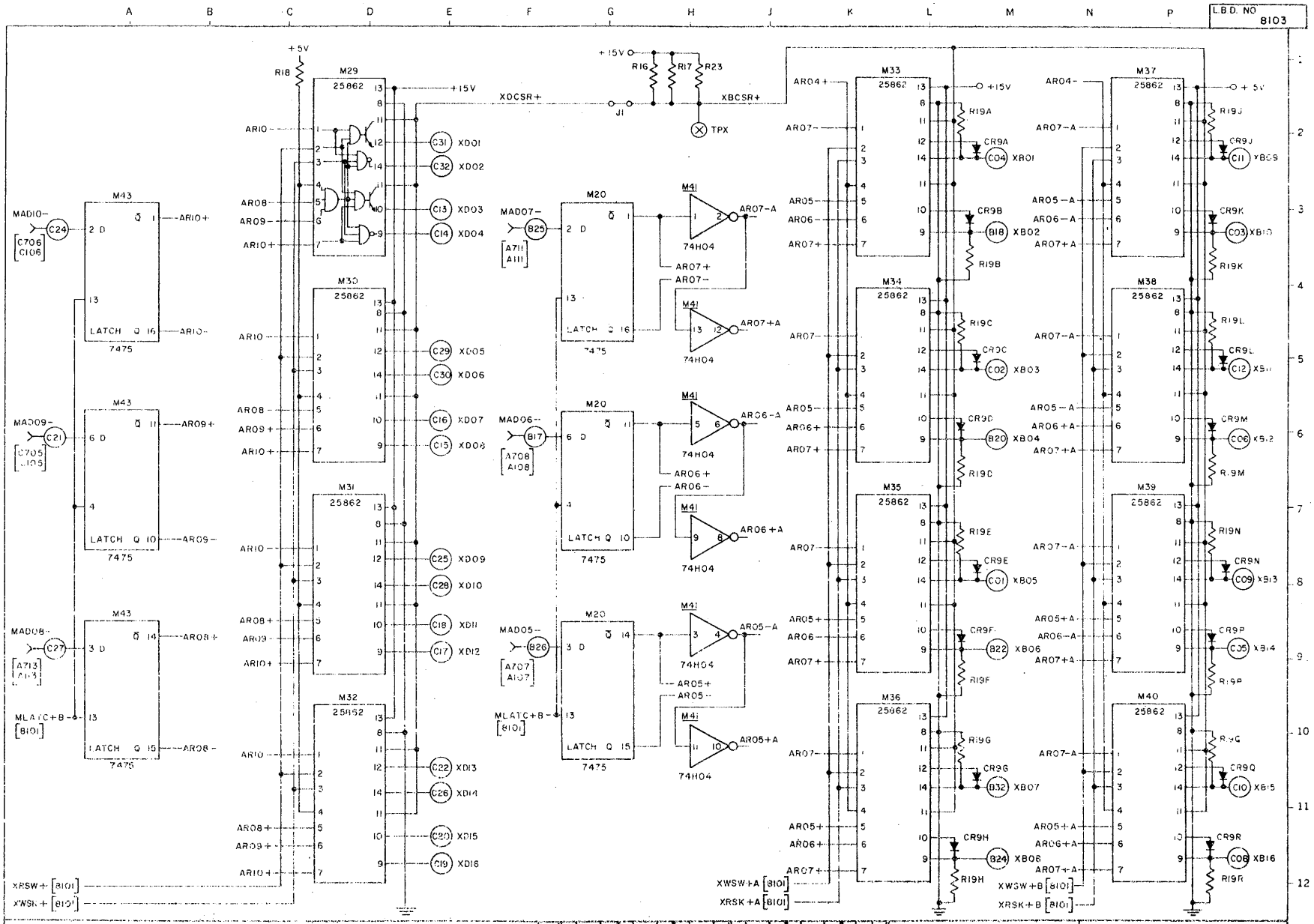
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. R. BOUDROT	DATE 8/10/72
ENG. S. DURVASULA	8/10/72
APP. D. ROTHENBERG	8/10/72
PROJECT NO. H404-01	

TITLE
CSM-150 MEMORY
Y SELECTION
CM-866 ADDRESS BOARD
SLOT 2

SIZE	DWG NO.	REV.
C	70032891	B

Form LBD F2760-571



NOTES:

1. DESIGNATES BOARD CONNECTOR AND PIN. >— INDICATES CSM-150 INTERFACE SIGNAL.
2. [ ] INDICATES SOURCE LBD OR I/O PIN.

REV	REVISIONS	CHK
A	PRE ISSUE	
B	ECO 807551 EXT. CMOS PER ECO 73-7-45	

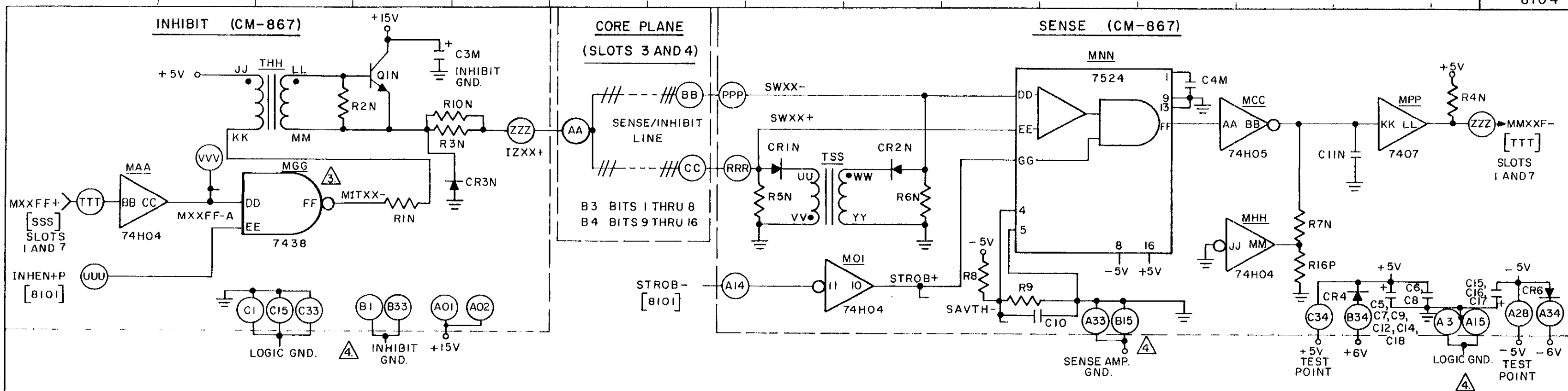
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham, Mass.

DR. A. BOUDROT	DATE 6/30/72	
ENG. S. DURVASULA	8/10/72	
APP. D. ROTHENBERG	8/10/72	
PROJECT NO. H404-01		

TITLE: CSM-150 MEMORY X SELECTION CM-866 ADDRESS BOARD SLOT 2

SIZE	DWG NO.	REV.
C	70032892	B

Form LBD F2760 571



CM867 SLOT	DATA BIT, MXXFF+, MXXFF-A, MITXX-, SWXX±, IZXX+, MMXXF-	COMPONENTS BUFFERED SIGNALS			INHIBIT																	CORE PLANE			SENSE																						
					DATA INPUT PINS		DIP MAA			BD. PINS	DIP MGG					XFMR. THH					INHIBIT PINS		SENSE PINS				XFMR. TSS					7524 DIP MNN					DIP MCC			DIP MHH			DIP MPP			DATA OUTPUT PINS	
							DIP	IN PIN	OUT PIN		DIP	BD. PIN	IN PINS		OUT PIN	XFMR	IN PINS		OUT PINS								XFMR	IN PINS		OUT PINS		DIP	IN PINS			OUT PIN	DIP	IN PIN	OUT PIN	DIP	IN PIN	OUT PIN	DIP	IN PIN	OUT PIN		
					VARIABLE																	VARIABLE			VARIABLE																						
	XX	M	N	P	SSS	TTT	AA	BB	CC	VVV	GG	UUU	DD	EE	FF	HH	JJ	KK	LL	MM	ZZZ	AA	BB	CC	PPP	RRR	SS	UU	VV	WW	YY	NN	DD	EE	GG	FF	CC	AA	BB	HH	JJ	MM	PP	KK	LL	ZZZ	TTT
5	01	A	A	A	C01	A06	1	03	04	A07	4	A12	04	05	06	1	05	12	11	06	B05	03	02	01	B04	B03	3	03	14	04	13	7	07	06	11	12	3	11	10	1	09	08	13	01	02	A19	A21
	02	A	B	A	C02	A04	1	01	02	A05	4	A12	01	02	03	1	07	10	09	08	B06	04	06	05	B08	B07	3	01	16	02	15	7	03	02	15	14	3	09	08	1	09	08	13	09	08	A25	A15
	03	B	C	A	C07	A08	1	05	06	A09	4	A12	10	09	08	1	03	14	13	04	B11	09	08	07	B10	B09	3	11	06	12	05	8	07	06	11	12	3	05	06	1	09	08	13	03	04	A21	A09
	04	B	D	A	C08	A10	1	13	12	A11	4	A12	12	13	11	1	01	16	15	02	B12	10	12	11	B14	B13	3	10	07	09	08	8	02	03	15	14	3	03	04	1	09	08	13	05	06	A23	A04
	05	C	E	B	C19	C25	2	13	12	–	5	C17	09	10	08	2	01	16	15	02	B29	29	32	31	B32	B31	4	11	06	12	05	9	07	06	11	12	15	03	04	2	05	06	14	03	04	C10	A03
	06	C	F	B	C20	C23	2	11	10	–	5	C17	12	13	11	2	03	14	13	04	B30	30	28	27	B28	B27	4	08	09	07	10	9	02	03	15	14	15	01	02	2	05	06	14	05	06	C06	C31
	07	D	G	B	C13	C21	2	01	02	–	5	C17	04	05	06	2	05	12	11	06	B23	23	26	25	B26	B25	4	03	14	04	13	10	07	06	11	12	15	05	06	2	05	06	14	01	02	C12	C30
	08	D	H	B	C14	C19	2	03	04	–	5	C17	02	01	03	2	07	10	09	08	B24	24	22	21	B22	B21	4	02	15	01	16	10	02	03	15	14	15	11	10	2	05	06	14	09	08	C08	C25
6	09	A	A	A	C29	A06	1	03	04	A07	4	A12	04	05	06	1	05	12	11	06	B05	03	02	01	B04	B03	3	03	14	04	13	7	07	06	11	12	3	11	10	1	09	08	13	01	02	A19	C22
	10	A	B	A	C28	A04	1	01	02	A05	4	A12	01	02	03	1	07	10	09	08	B06	04	06	05	B08	B07	3	01	16	02	15	7	03	02	15	14	3	09	08	1	09	08	13	09	08	A25	C21
	11	B	C	A	C23	A08	1	05	06	A09	4	A12	10	09	08	1	03	14	13	04	B11	09	08	07	B10	B09	3	11	06	12	05	8	07	06	11	12	3	05	06	1	09	08	13	03	04	A21	C16
	12	B	D	A	A05	A10	1	13	12	A11	4	A12	12	13	11	1	01	16	15	02	B12	10	12	11	B14	B13	3	10	07	09	08	8	02	03	15	14	3	03	04	1	09	08	13	05	06	A23	C15
	13	C	E	B	A06	C25	2	13	12	–	5	C17	09	10	08	2	01	16	15	02	B29	29	32	31	B32	B31	4	11	06	12	05	9	07	06	11	12	15	03	04	2	05	06	14	03	04	C10	C10
	14	C	F	B	A19	C23	2	11	10	–	5	C17	12	13	11	2	03	14	13	04	B30	30	28	27	B28	B27	4	08	09	07	10	9	02	03	15	14	15	01	02	2	05	06	14	05	06	C06	C09
	15	D	G	B	A17	C21	2	01	02	–	5	C17	04	05	06	2	05	12	11	06	B23	23	26	25	B26	B25	4	03	14	04	13	10	07	06	11	12	15	05	06	2	05	06	14	01	02	C12	C04
	16	D	H	B	A23	C19	2	03	04	–	5	C17	02	01	03	2	07	10	09	08	B24	24	22	21	B22	B21	4	02	15	01	16	10	02	03	15	14	15	11	10	2	05	06	14	09	08	C08	C03

NOTES:

4. LOGIC, INHIBIT AND SENSE AMP. GNDS. ARE TIED TOGETHER BY THE BACKPLANE GND. BUS.

3. M, N, P, DOUBLE AND TRIPLE LETTERS ARE VARIABLES SHOWN IN TABLE. AN EXAMPLE FOR INHIBIT VARIABLES GG, FF, XX AND N IS THE MITO1– CONNECTION FROM DIP M4 OUTPUT 06 TO RESISTOR R1A.

2. SPARE GATES: M3 OUTPUTS 2 AND 12, M11 OUTPUT 12, M13 OUTPUTS 10 AND 12

1. ◯ DESIGNATES BOARD CONNECTOR AND PIN. >— INDICATES CSM-150 INTERFACE SIGNAL. [ ] INDICATES SOURCE LBD OR I/O PIN

REVISIONS: REV. A; B — ECO 30795; EXT. CHGS PER E.C.O. 73/15

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

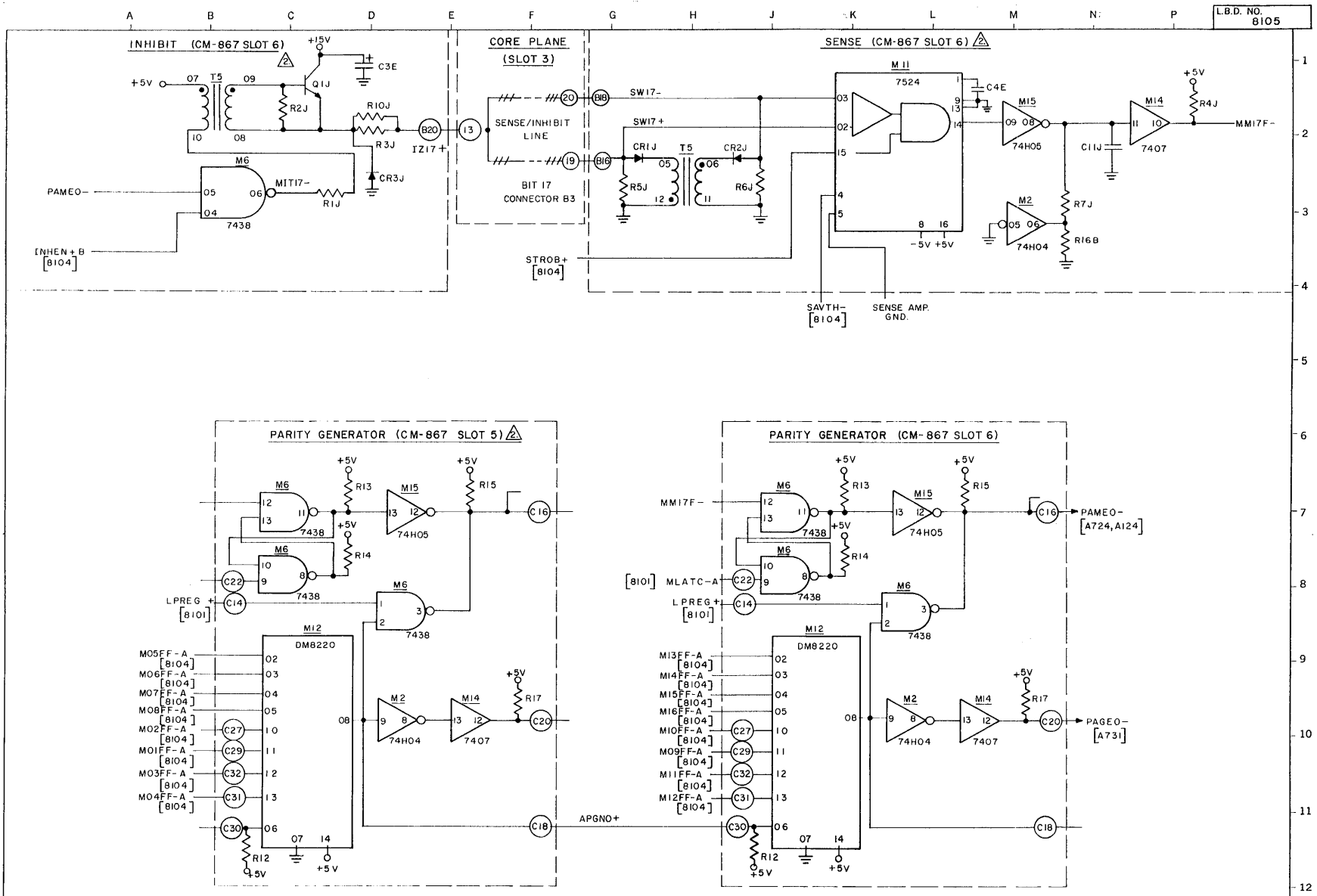
DR. R. BOUDROT	DATE
ENG. S. DURVASULA	8/10/72
APP. D. ROTHENBERG	8/10/72
PROJECT NO. H404-01	

TITLE: CSM-150 MEMORY DATA BITS 1 THRU 16 CM-867 SLOTS 5 AND 6

SIZE C | DWG NO. 70032893 | REV. B

L.B.D. NO. 8104

Form LBD F2760-571



NOTES:

△

△

2 CM-867 SLOT 5 HAS SPARE INHIBIT, SENSE AND PARITY CIRCUITS.

1 ○ DESIGNATES BOARD CONNECTOR AND PIN. >— INDICATES CSM-150 INTERFACE SIGNAL. [ ] INDICATES SOURCE LBD OR I/O PIN

REVISIONS	REV.	CHK
PER ISSUE	A	
ECO 30795 ECT 6985 PER ECO 73-7-5	B	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

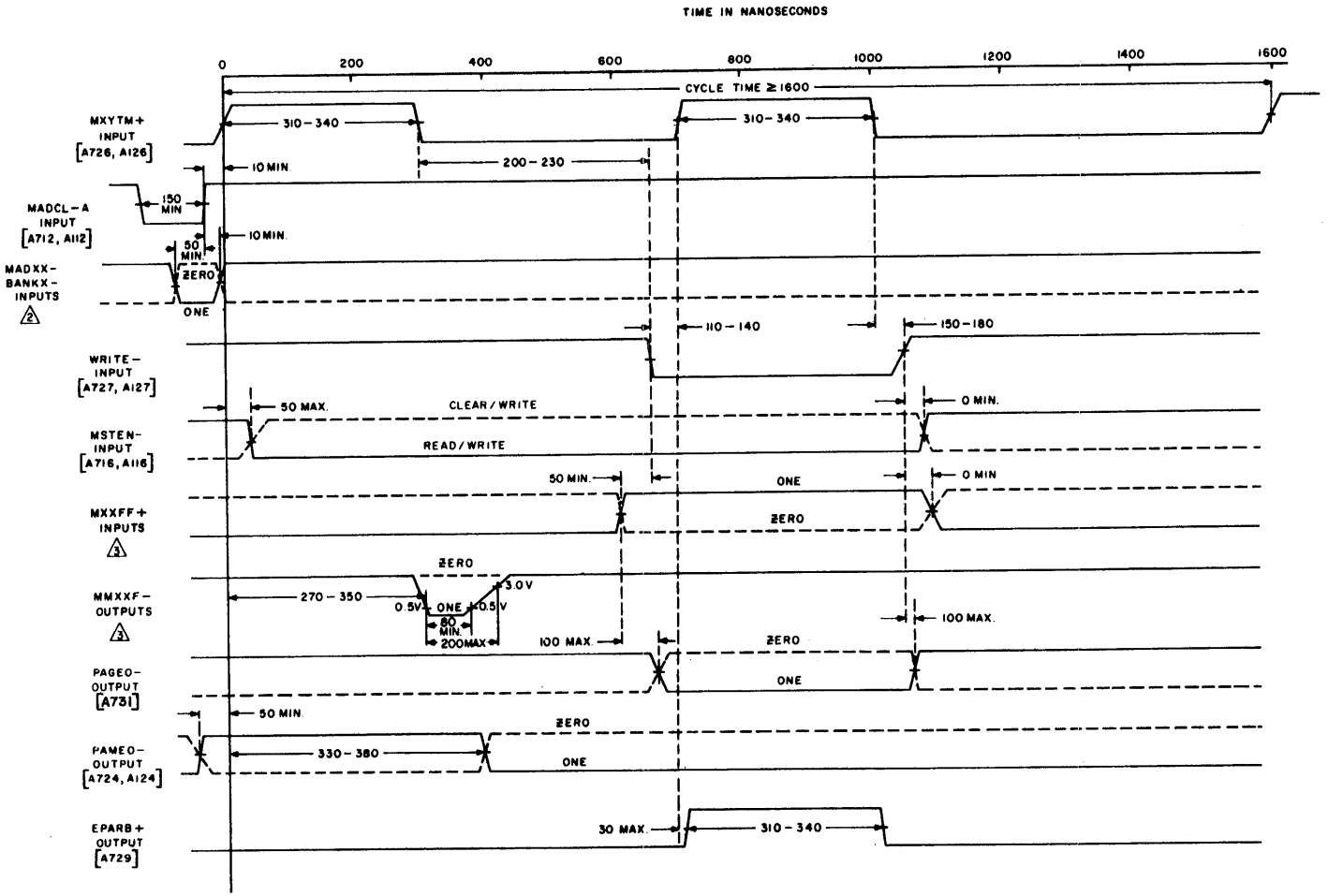
DR. R. BOUDROT	DATE 8/10/72
ENG. S. DURVASULA	8/10/72
APP. D. ROTHENBERG	8/10/72
PROJECT NO. H404-01	

TITLE
CSM-150 MEMORY
PARITY
CM-867 SLOTS 5 AND 6

SIZE	DWG NO.	REV.
C	70032894	B

L.B.D. NO. 8105

Form LBD F2760-571



NOTES:

△

3 SEE LBD 8104 FOR INTERFACE PINS.

2 SEE LBD 8101 FOR INTERFACE PINS.

1 TIME IN NANOSECONDS MEASURED AT CSM-150 BACKPLANE AND 1.5V POINTS, UNLESS OTHERWISE SPECIFIED.

REV	REVISIONS	CHK	PER ISSUE
A	ECO 30195 12 EXT CHGS PER ECO 73-7-5		
C	ECO 30996		73-12-11

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass

DR. R. BOUDROT	DATE 8/10/72	
ENG. S. DURVASULA	8/10/72	
APP. D. ROTHENBERG	8/10/72	
PROJECT NO. H404-01		

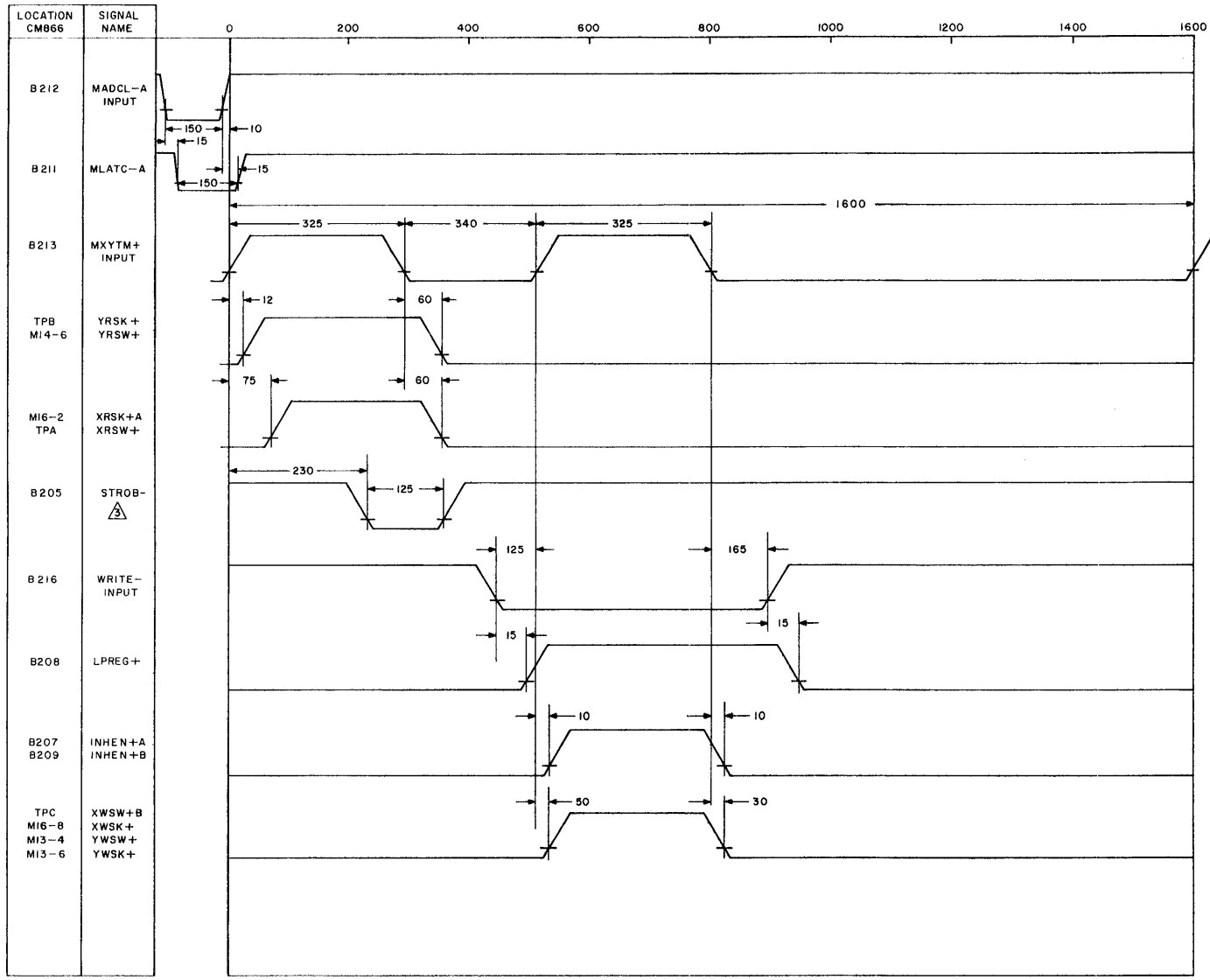
TITLE: CSM-150 MEMORY INTERFACE TIMING

SIZE C | DWG NO. 70032895 | REV. C

Form LBD F2760-571

L.B.D. NO. 8111

TIME IN NANOSECONDS



NOTES:

△

3 JUMPERS J2 AND J3 SHALL VARY STROBE TIMING 12±3 NS EARLIER AND LATER RESPECTIVELY.

2 INPUTS NOT SHOWN AND OUTPUTS SHALL BE PRE LBD 8110.

1 TIME IN NANOSECONDS (1.5V POINTS). TOLERANCE ±8NS.

CHK.	REVISIONS	REV.
	PER ISSUE A	
	ECO 30795 B EXT. CHGS PER ECO 73-7-5 ECO 74-4-4	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. W. OBRIEN	DATE 8/10/72
ENG. S. DURVASULA	8/10/72
APP. D. ROTHENBERG	8/10/72
PROJECT NO. H404-01	

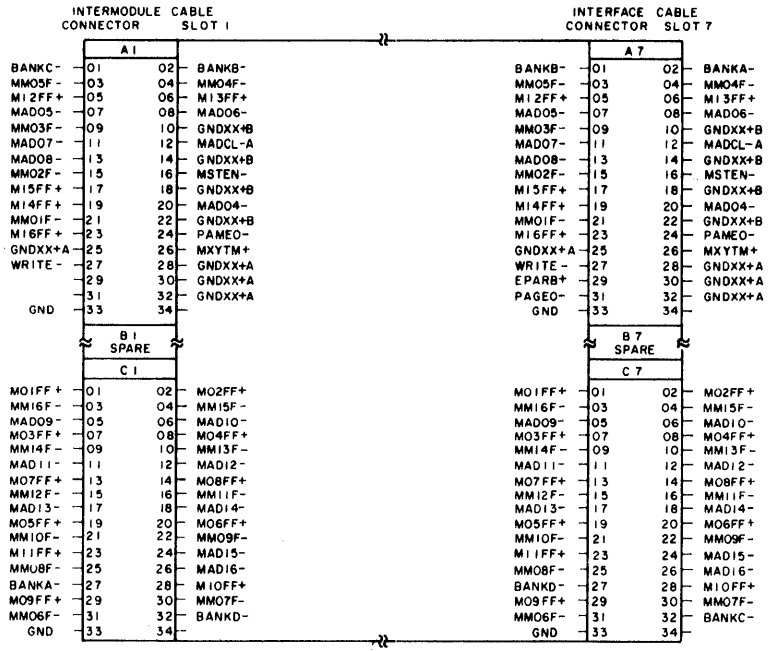
TITLE
CSM-150 MEMORY
INTERNAL TIMING
DIAGRAM

SIZE	DWG NO.	REV.
C	70032897	B

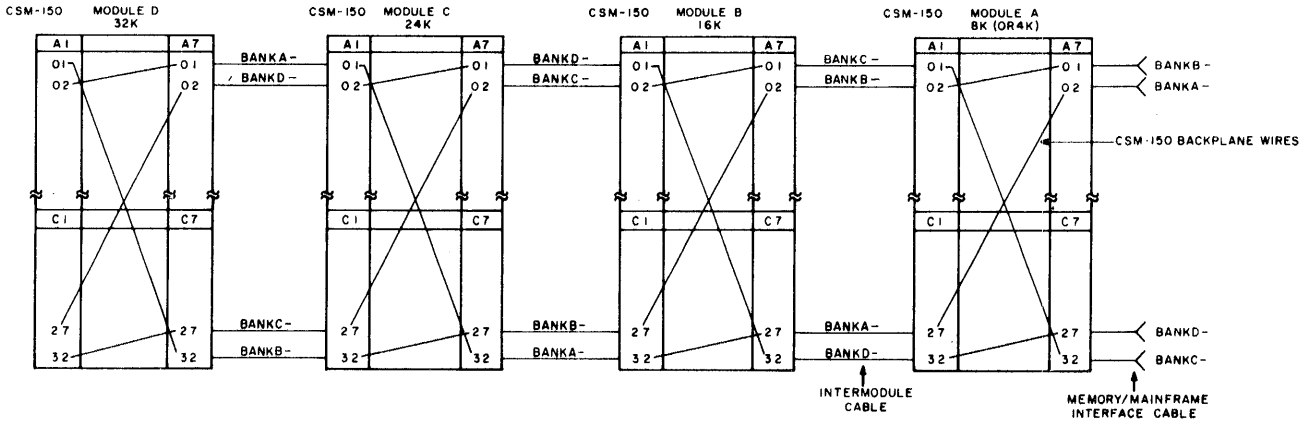
Form LBD F2760-571

L.B.D. NO. 8112

MEMORY/MAINFRAME INTERFACE (2)



BANK SELECT WIRING (1)



NOTES:

(1) BANKX- IS WIRED FROM A702 TO A227. BACKPLANE WIRES SHOWN ALLOW THE PROPER BANK SELECT SIGNAL TO BE CONNECTED TO EACH CSM-150 MODULE.

(2) INTERFACE WIRING IS IDENTICAL FOR ALL CSM-150 MODULES. BANKX- SIGNAL NAMES ARE SHOWN FOR MODULE A AND DIFFERENCES FOR MODULES B, C, D SHOWN IN THE LOWER DIAGRAM.

REV	REVISIONS	PER	ISSUE
A	ECO 30735 REV B EXT CNGS PER ECO 73-7-5 ECO 30996 REV C	ECO 30996	73-12-11

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. R. BOUDROT	DATE 6/10/72
ENG. S. DURVASULA	6/10/72
APP. D. ROTHENBERG	6/10/72
PROJECT NO. H404-01	

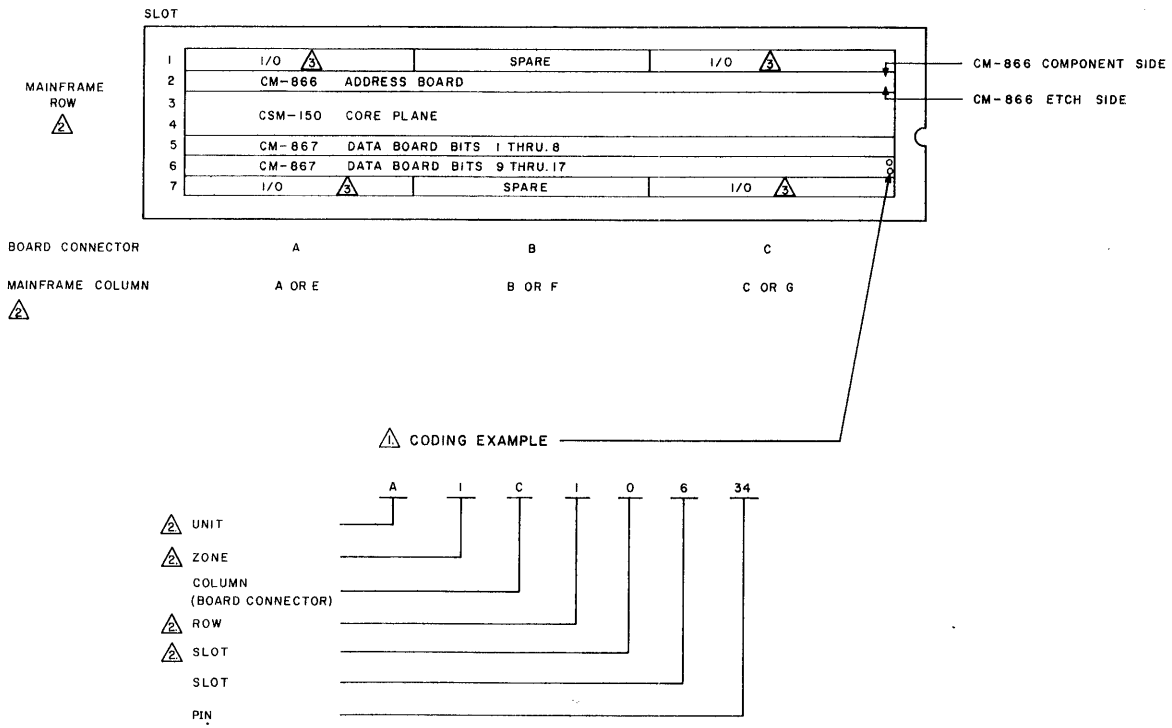
TITLE: CSM-150 MEMORY I X 3 CONNECTOR WIRING

SIZE C | DWG NO. 70032896 | REV. C

Form LBO F2760-571

L.B.D. NO. 8113

PAC ALLOCATION VIEWED FROM PAC SIDE



NOTES:

(3) SLOT 7 ACCOMODATES TWO INPUT CABLES. SLOT 1 IS FOR TWO INTERMODULE JUMPER CABLES.

(2) CHARACTERS ARE OPTIONAL AT MEMORY MODULE LEVEL AND GENERALLY NOT USED, FOR EXAMPLE, AIC10634 IS SHORTENED TO C634 TO INDICATE SLOT 6 CONNECTOR C PIN 34.

(1) SEE H316 CODING DWG. 70023412 FOR ADDITIONAL DETAILS.

REV.	REVISIONS	CHK.
A	PRE ISSUE	
B	ECO 30795 ENT CHGS PER ECO 73-75	

—	P70 032 899

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

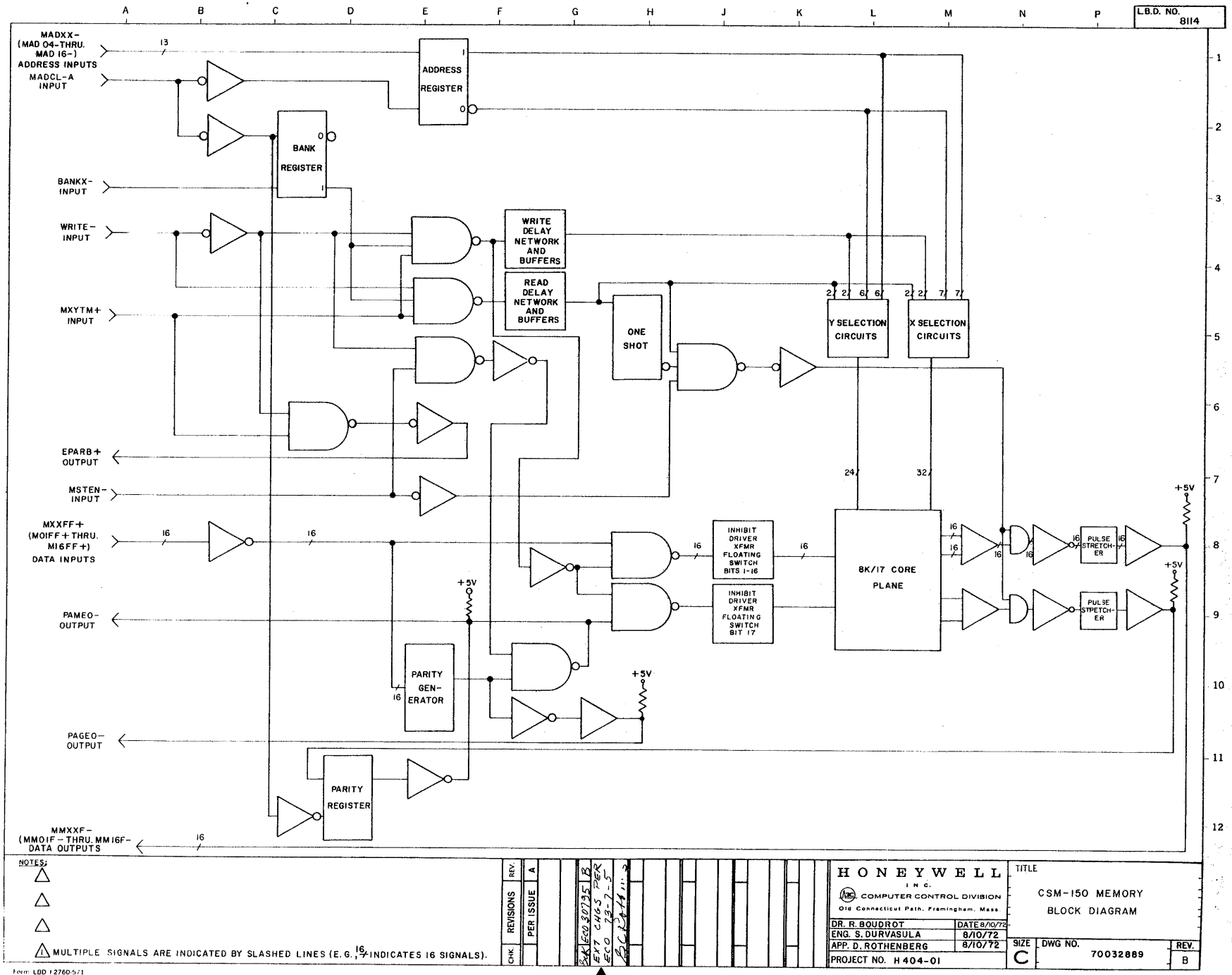
DR.	R. BOUDROT	DATE 8/10/72
ENG.	S. DURVASULA	8/10/72
APP.	D. ROTHENBERG	8/10/72
PROJECT NO.	H 404-01	

PARTS LIST

TITLE: CSM-150 MEMORY
PAC COMPLEMENT/ALLOCATION

SIZE	DWG NO.	REV.
C	70032899	B

Form LBD F2760-571


L.B.D. NO. 8114
MADXX- (MAD 04- THRU. MAD 16-) ADDRESS INPUTS
MADCL-A INPUT
ADDRESS REGISTER
BANK REGISTER
BANKX- INPUT
WRITE- INPUT
WRITE DELAY NETWORK AND BUFFERS
READ DELAY NETWORK AND BUFFERS
MXYTM+ INPUT
ONE SHOT
Y SELECTION CIRCUITS
X SELECTION CIRCUITS
EPARB+ OUTPUT
MSTEN- INPUT
MXXFF+ (M01FF+ THRU. M16FF+) DATA INPUTS
INHIBIT DRIVER XFMR FLOATING SWITCH BITS 1-16
INHIBIT DRIVER XFMR FLOATING SWITCH BIT 17
8K/17 CORE PLANE
PULSE STRETCHER
+5V
PAMEO- OUTPUT
PARITY GEN- ERATOR
PAGEO- OUTPUT
PARITY REGISTER
MMXXF- (MM01F- THRU. MM16F- DATA OUTPUTS
NOTES:
MULTIPLE SIGNALS ARE INDICATED BY SLASHED LINES (E.G. 16/ INDICATES 16 SIGNALS).
REVISIONS
REV. A
PER ISSUE
CHK.
B ECO 30735 EXT CHGS PER ECO 73-7-5
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass
DR. R. BOUDROT DATE 8/10/72
ENG. S. DURVASULA 8/10/72
APP. D. ROTHENBERG 8/10/72
PROJECT NO. H 404-01
TITLE
CSM-150 MEMORY BLOCK DIAGRAM
SIZE C
DWG NO. 70032889
REV. B
Form LBD 12760-5/71

SECTION 10
MEMORY PAC DESCRIPTIONS

This section contains the following circuit descriptions and parts lists for the special Address Board, Model CM-866, and Data Board, Model CM-867, used in the CSM-150 Core Memory Module. For board locations, refer to the PAC complement, shown in LBD 8113, Drawing No. 70032899, in Section 9.

INTEGRATED CIRCUIT DESCRIPTIONS

The majority of integrated circuits are standard devices listed in vendor catalogs. Reference information is also contained in System 700, Type 716, Integrated Circuits Manual, Doc. No. 70130072667, which may be ordered from Honeywell Inc.

RECOMMENDED SPARE PARTS

One CM-866 address board, one CM-867 data board, and one CSM-150 core plane are recommended as spares.

ADDRESS BOARD, MODEL CM-866

The Address Board, CM-866, contains circuitry to perform the following functions.

a. Store bank enable and address inputs received from the processor. This is implemented with four 7475-quad latches. The latch circuit outputs in turn drive the 25862 selection drivers.

b. Provide selection and drive currents for an 8K matrix. This is implemented with twenty 25862-dual in-line packages, each of which includes two sink-switch pairs with decoding.

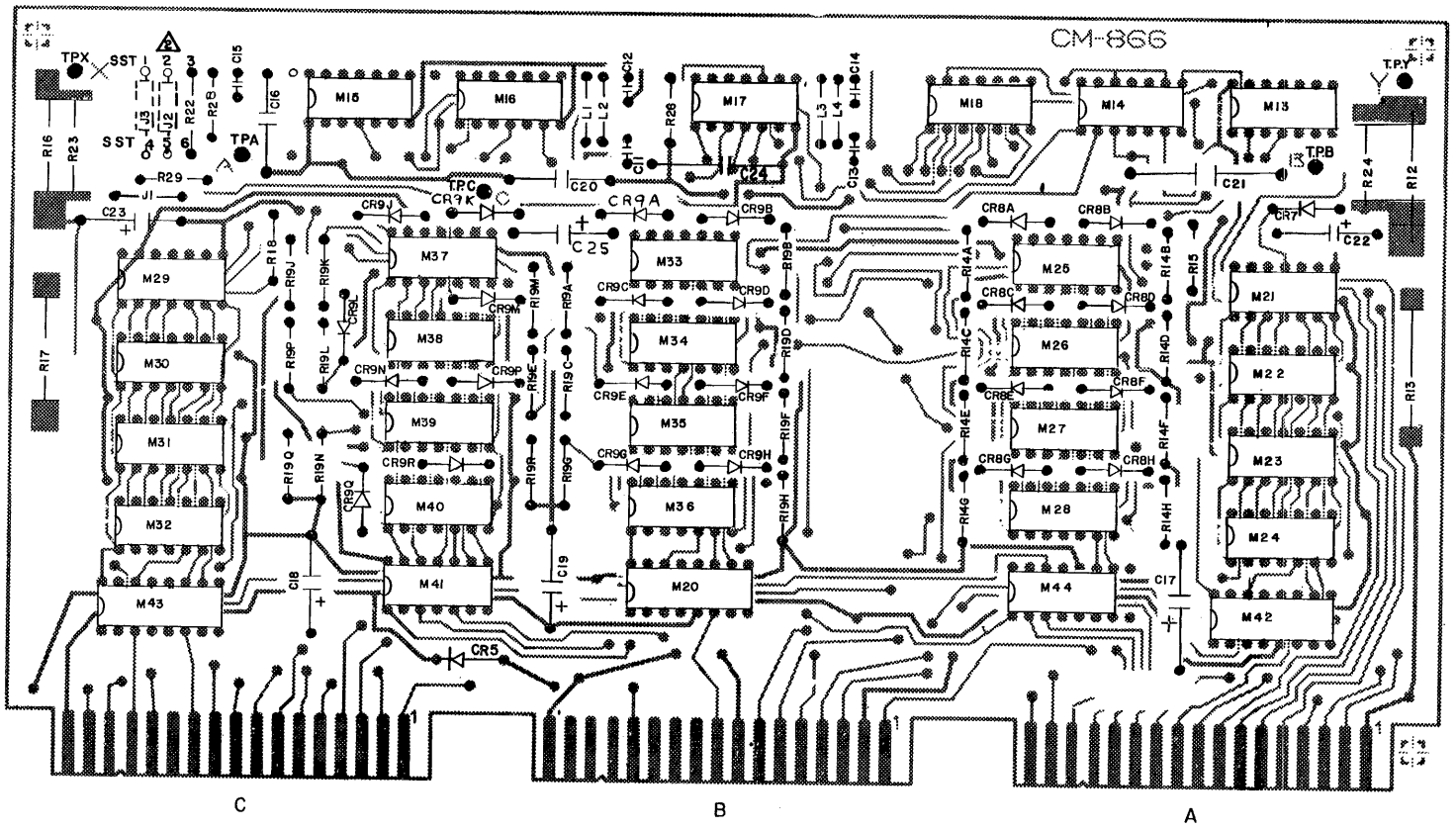
c. Provide logic and timing circuitry to control matrix read-write timing, inhibit timing, register latch timing, sense amplifier strobe generation (pulse width control and leading edge adjustment), load parity register timing, and parity error strobe pulse. LBDs 8101, 8102, and 8103, Drawing No. C70032890, C70032891, and C70032892, respectively, in Section 9 illustrate the schematics for the CM-866 address board. Figure 3-10-1 is the assembly drawing for the CM-866 and Table 3-10-1 contains a listing of parts.

Specifications are as follows:

a. Input Loading -- One standard TTL unit load except for MXYTM+, WRITE- and MADCL-A, which are two unit loads each.

b. Selection Output Characteristics -- Current: 480 mA, max.; voltage: 17.5V, max.

c. Timing -- Refer to LBDs 8110 and 8111, Drawing No. C70032895 and C70032897, respectively, in Section 9.



2. INSTALL J2 OR J3 TEMPORARILY AT SYSTEM TEST IF REQUIRED FOR STROBE MARGIN CHECK PER LBD 8101.

1. POWER RESISTORS R12,13,16,17,23,24. WILL BE MOUNTED OFF P.C. BD. NOT TO EXCEED THE COMPONENT HEIGHT SPEC. OF .230 MAX.

Figure 3-10-1. Address Board, Model CM-866, Assembly
(Drawing No. C70050523, Rev A)

Table 3-10-1.
Address Board, Model CM-866, Parts List
(P70050523, Rev C)

ITEM NO.		DOCUMENT NO.	DESCRIPTION	QTY 701
06	A	70950118 010	INTEGRATED DEVICE 74H00 M14	001
07	A	70950118 013	INTEGRATED DEVICE 74H10 M17	001
08	A	70950104 009	INTEGRATED DEVICE 9601 M15	001
09	A	70950118 011	INTEGRATED DEVICE 74H04 M13,M41,M18,M16	004
10	A	70950118 006	INTEGRATED DEVICE 7475 M44,M20,M42,M43	004
11	A	P04040854-002	INTEGRATED DEVICE 25862 M21 THRU M40	020
12	A	70943083 003	DIODE SILICON CR7,CR8A THRU CR8H CR9A THRU CR9R	025
13	C	70032890 000	ELE SCHMATIC REF DWG	REF
14	C	70032891 000	ELE SCHMATIC REF DWG	REF
15	C	70032892 000	ELE SCHMATIC REF DWG	REF
16	A	70930004 134	CAPACITOR 10 PF 6/-5%	002

NOTES

NOTE 1 ASSEMBLE PER C70050523
701 - CM-866

NOTE 2 VALUE MAY CHANGE AT FINAL TEST
RANGE 4.7K 70932114065 TO 12.0K 70932114075

Table 3-10-1. (Cont)

ITEM NO.	DOCUMENT NO.	DESCRIPTION	QTY
			701
		C13,C14	
17 A	70932226 259	RESISTOR FIXED W/W 40.2 OHMS 6/-1% 3WNI R12,R13,R16,R17	004
18 A	70932004 029	RESISTOR 150 OHMS 1/2W 6/-5% R24	001
19 A	70932114 049	RESISTOR 1.0K OHM 1/4W 6/-2% R15,R18,R26	027
		R14A THRU R14H R19A THRU R19R	
#20 P	04420034 001	DIODE SI RECT CR5	001
21 A	70939207 025	COIL RF 10UH 6/-10% L1,L2,L3,L4	004
22 A	70930100 208	CAPACITOR .01MFD 6/-20% C21,C24,C20,C16	004
23 A	70930004 112	CAPACITOR 62PF 6/-5% C11,C12	002
24 A	70930230 023	CAPACITOR 6.8MFD 6/-2% 25V C22,C23,C17,C18,C19 C25	006
25 A	70932114 070	RESISTOR 7.5K OHMS 1/4W 6/-2% R22 NOTE 2	001
26 A	70930004 106	CAPACITOR 35 PF 6/-5% C15	001
27 A	70932114 047	RESISTOR 820 OHMS 1/4W 6/-2% R28	001
28 A	70932114 075	RESISTOR 12.K OHMS 1/4W 6/-2% R29	001
29 A	70937077 004	TERMINAL STUD T.P.X,T.P.Y, T.P.A, T.P.B,T.P.C	005
30 A	70937010 001	TERMINAL STUD SST1 THRU SST6	006
31 A	04910040 004	JUMPER J1	001
32 A	70932004 026	RESISTOR 110 OHMS 1/2W 6/-5% R23	001
33 B	70008913 866	PLATE IDENT.	001

DATA BOARD, MODEL CM-867

The CM-867 data board contains circuitry to implement the following functions:

a. Amplify sense winding signals for 9 bits and adapt them for presentation to the central processor.

b. Generate inhibit currents for 9 bits, depending upon the state of the data input lines to the board.

c. Provide parity generation. Store the sense output of the parity bit in the parity data register.

d. Reduce the +6V and -6V power supply levels to +5V and -5V, respectively, for use with TTL circuits.

The schematics for the CM-867 data board are shown in LBDs 8104 and 8105, Drawing No. 70032893 and 70032894, respectively, in Section 9. The assembly drawing for the CM-867 data board is shown in Figure 3-10-2, and the associated parts list is presented in Table 3-10-2.

Specifications are as follows:

a. Sense Input -- ONE: 25 mV minimum for 30 ns; ZERO: 12 mV max. for the duration of strobe.

b. Inhibit Output -- Max. current: 850 mA; max. voltage: 17V

c. Timing -- See LBDs 8110 and 8111, Drawing No. 70032895 and C70032897, respectively, in Section 9.

CSM-150 CORE PLANE

The CSM-150 plug-in core plane is a conventional 3-wire, 3D, coincident current configuration. Cores are switched by controlling currents in two orthogonal wires threaded through the cores, called X- and Y-lines. The sense and inhibit functions are shared by the third line that is parallel to the Y-line. A current through the sense-inhibit line during the write portion of a cycle prevents the core plane from switching and thus controls whether a ONE or ZERO is written into the core plane. The flux change during the read time is also sensed on the sense-inhibit wire during read-write cycles. There are 17 mats, each containing 8192 cores, for a total of 8192 words, each 17 bits long (parity is included).

The core plane assemblies vary according to the manufacturer, but all have the same interface characteristics. Figures 3-10-3 and 3-10-4 illustrate the assembly. Figure 3-10-3 is a simplified schematic diagram of the CSM-150 core plane, and Figure 3-10-4 illustrates the interface connections of the CSM-150 core plane.

Specifications are as follows:

Core O.D. = 18 mils

Core signals at nominal drive (400 mA) and inhibit (375 mA) currents:

Min. ONE: 25 mV for 30 ns

Max. ZERO: 12 mV

Temperature Compensation: 0.25 percent per °C

Peaking Time: 180 ns typical

Switching Time: 290 ns max.

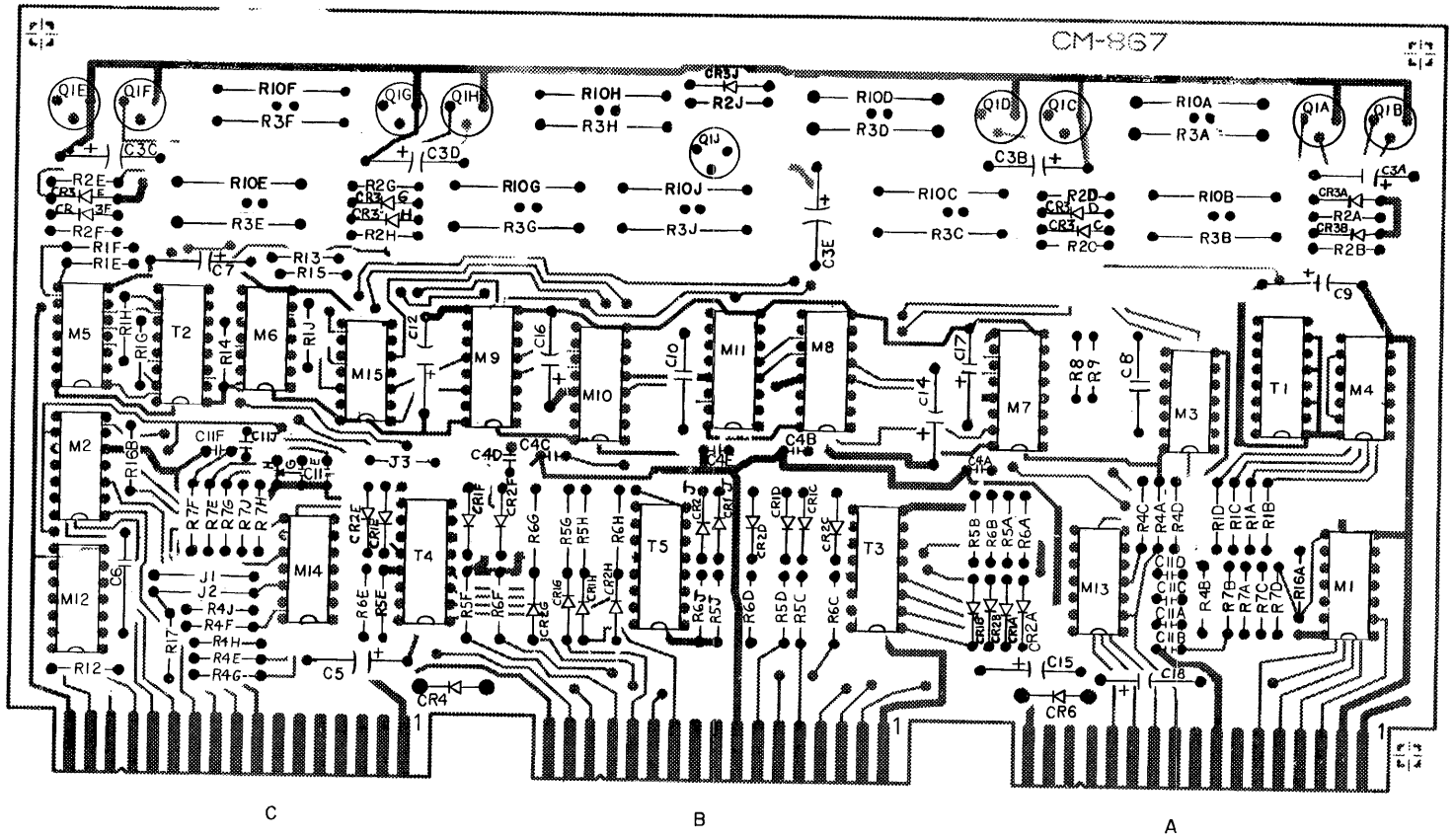


Figure 3-10-2. Data Board, Model CM-867, Assembly
(Drawing No. C70050524, Rev B)

Table 3-10-2.
Data Board, Model CM-867, Parts List
(P70050524, Rev C)

ITEM NO.		DOCUMENT NO.	DESCRIPTION	QTY 701	702
06	A	70950118 011	INTEGRATED DEVICE 74H04 M1,M2	002	002
07	A	70950118 019	INTEGRATED DEVICE 7438 M4,M5,M6	003	003
08	A	70950100 044	INTEGRATED DEVICE 7524 M7 THRU M11	005	005
09	A	70938024 001	TRANSFORMER DIP T1 THRU T5	005	005
10	A	70943778 001	TRANSISTOR NPN Q1A THRU Q1J	009	009
11	A	70943083 003	DIODE SILICON CR1A THRU CR1J CR2A THRU CR2J CR3A THRU CR3J	027	027
12	C	70032893 000	ELE SCHMATIC REF DWG	REF	REF
13	C	70032894 000	ELE SCHMATIC REF DWG	REF	REF
15	A	70916400 002	INSULATOR DISK	009	009
16	A	70932114 029	RESISTOR 150 OHMS 1/4W 5/-2% R2A THRU R2J R5A THRU R5J R6A THRU R6J	027	027
17	A	70932226 245	RESISTOR FIXED W/W	018	018

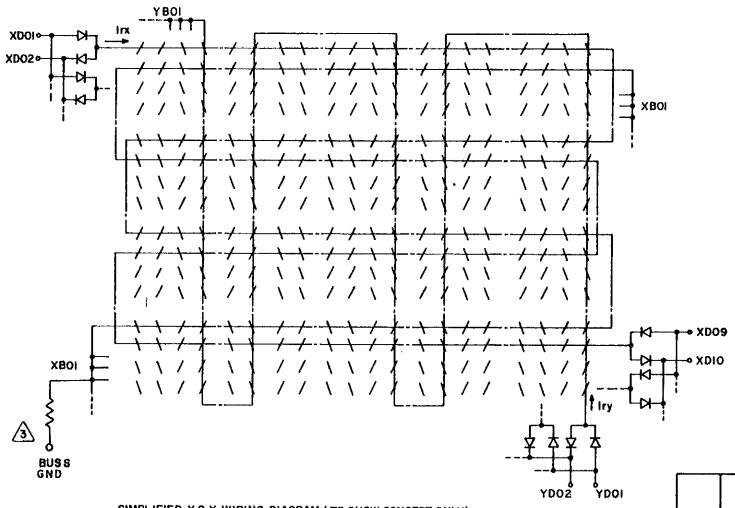
NOTES

ASSEMBLE PER C70050524
701 - CM-867

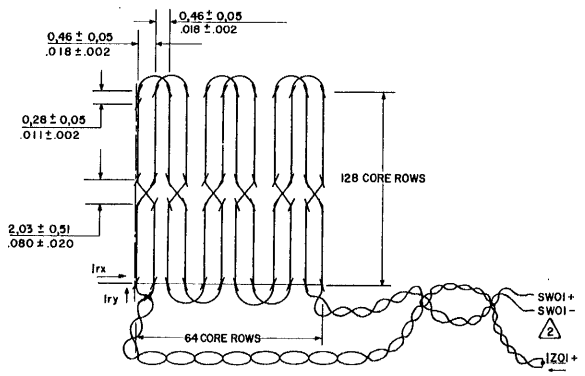
702=CM-867A

Table 3-10-2. (Cont)

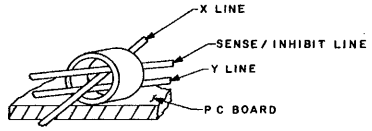
ITEM NO.		DOCUMENT NO.	DESCRIPTION	QTY 701	702
18	A	70932114 001	28.7 OHMS &/-1% 3WNI R3A THRU R3J, R10A THRU R10J RESISTOR	001	001
19	A	70932114 060	10 OHM &/-2% 1/4W R9 RESISTOR	001	001
20	A	70930230 023	3K OHM &/-2% 1/4W R8 CAPACITOR	014	014
21	A	70930100 208	6.8 MFD &/-20% 25V C3A THRU C3E,C5,C7, C9,C12,C14,C15, C16,C17,C18 CAPACITOR	003	003
22	A	70930004 019	.01MFD &/-20% C6,C10,C8 CAPACITOR	005	005
23		70930004 012	120PFD &/-10% C4A THRU C4E CAPACITOR	009	009
24	A	04040405 001	62 PF &/-10% C11A THRU C11J INTEGRATED DEVICE	001	001
25	A	70950118 032	DM8220N M12 INTEGRATED DEVICE	002	002
26	A	70950118 050	7407 M13,M14 INTEGRATED DEVICE	002	002
■27	P	04420034 001	74H05 M3,M15 DIODE SI RECT	002	002
28	A	70932114 017	CR4,CR6 RESISTOR	009	009
29	A	70932114 056	47 OHM 1/4W &/-2% R1A THRU R1J RESISTOR	025	025
31	A	04910040 004	2K OHM 1/4W &/-2% R4A THRU R4J R13 THRU R15 R7A THRU R7J R16A-B R17, R12 JUMPER	003	003
32	B	70008913 86,	J1,J2,J3 PLATE IDENT	001	
33	B	70025642867	PLATE IDENT		001
34		70940001-020	WIRE ELEC TIN-24AWG		A/R



SIMPLIFIED X & Y WIRING DIAGRAM (TO SHOW CONCEPT ONLY)



SIMPLIFIED INHIBIT/SENSE WIRING DIAGRAM FOR TYPICAL BIT (BIT 1)



TYPICAL WIRE LAY

8K STACK

X-DECODE 8K

XD	READ CA	WRITE CC	XB 01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16
	01	02	0	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
	03	04	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
	05	06	32	34	36	38	40	42	44	46	48	50	52	54	56	58	60	62
	07	08	33	35	37	39	41	43	45	47	49	51	53	55	57	59	61	63
	09	10	64	66	68	70	72	74	76	78	80	82	84	86	88	90	92	94
	11	12	65	67	69	71	73	75	77	79	81	83	85	87	89	91	93	95
	13	14	96	98	100	102	104	106	108	110	112	114	116	118	120	122	124	126
	15	16	97	99	101	103	105	107	109	111	113	115	117	119	121	123	125	127

Y-DECODE 8K

YD	READ CA	WRITE CC	YB 01	02	03	04	05	06	07	08
	01	02	0	1	4	5	8	9	12	13
	03	04	2	3	6	7	10	11	14	15
	05	06	16	17	20	21	24	25	28	29
	07	08	18	19	22	23	26	27	30	31
	09	10	32	33	36	37	40	41	44	45
	11	12	34	35	38	39	42	43	46	47
	13	14	48	49	52	53	56	57	60	61
	15	16	50	51	54	55	58	59	62	63

WORST CASE PATTERN 8K

	Y0							Y63
X0	1	0	1	0	1	0	1	0
	1	0	1	0	1	0	1	0
	1	0	1	0	1	0	1	0
X63	1	0	1	0	1	0	1	0
X64	0	1	0	1	0	1	0	1
	0	1	0	1	0	1	0	1
	C	1	0	1	0	1	0	1
X127	0	1	0	1	0	1	0	1

NOTE:

1. CA DENOTES DIODE ANODE BUS
   CC DENOTES DIODE CATHODE BUS
2. INHIBIT PAIRS SHALL BE TWISTED TOGETHER WITH SENSE PAIRS FOR A GIVEN BIT AS SHOWN, OR THE INHIBIT WIRES SHORTED AT THE CORE MAT AND A TWISTED TRIPLET USED FROM THE CORE MAT TO THE INTERFACE CONNECTOR.
3. ARTWORK PROVISIONS SHOULD BE MADE FOR 24 1/4 WATT RESISTORS FOR THE 8K H-716. THEY ARE NOT NEEDED FOR THE CSM-150 (8K H-716) AND MAY NOT BE NEEDED FOR THE 8K H-716.

Figure 3-10-3. Simplified Schematic Diagram of the CSM-150 Core Plane (Drawing No. D70033040, Rev C)

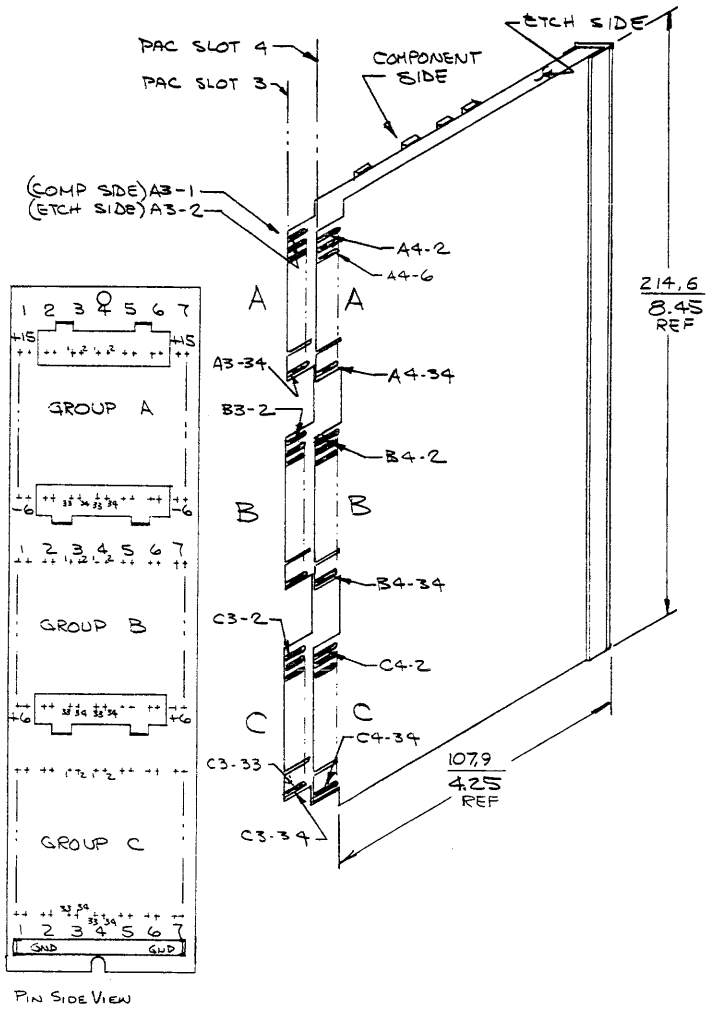
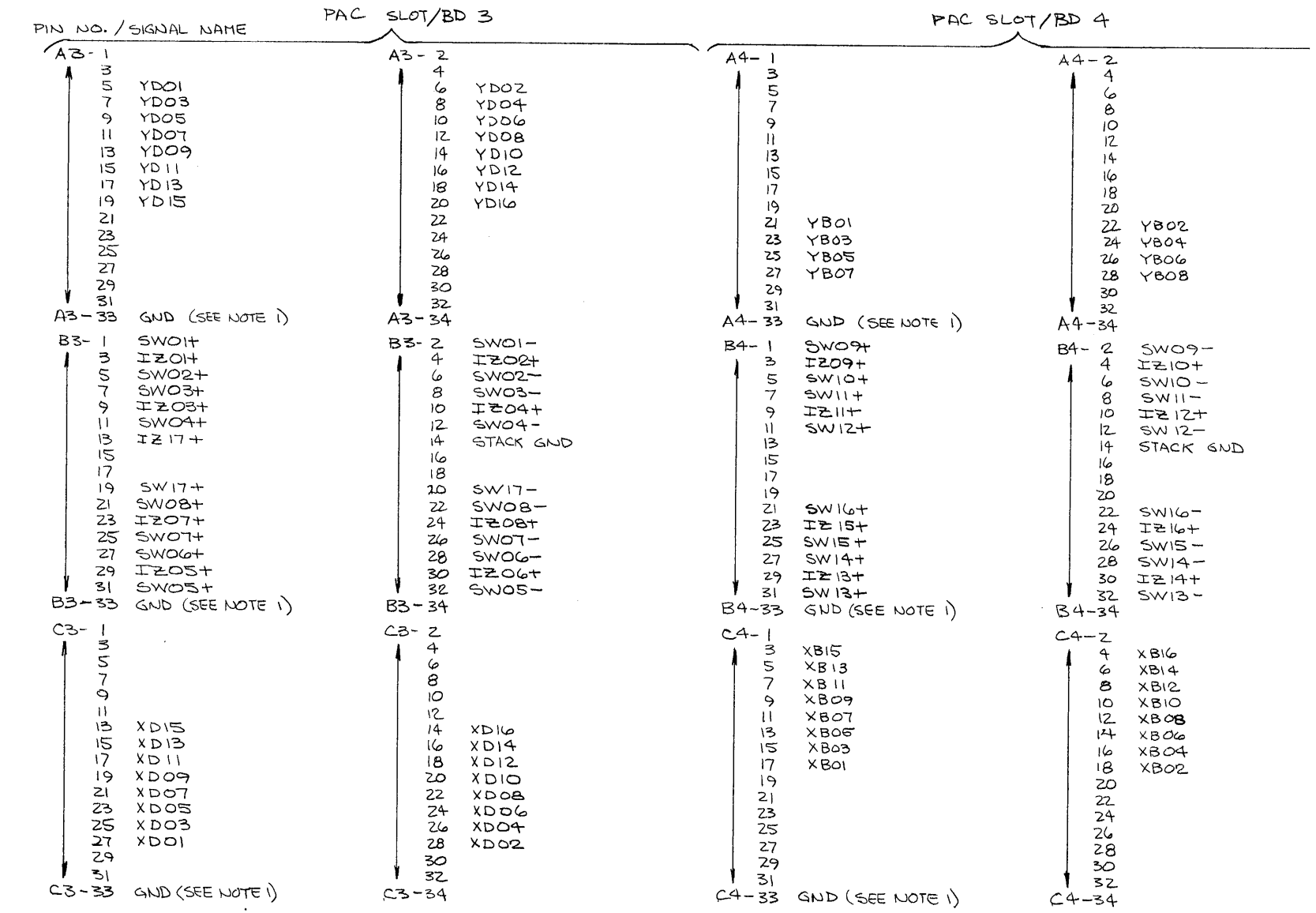


Figure 3-10-4. Interface Connections of the CSM-150 Core Plane (Drawing No. C70032758, Rev A) (Sheet 1 of 2)



NOTES

1. BACKPLANE GROUND SHOWN FOR REFERENCE. "STACK GND" SHOULD NOT BE TIED TO THESE PINS BY VENDOR

Figure 3-10-4. Interface Connections of the CSM-150 Core Plane (Drawing No. C70032758, Rev A) (Sheet 2 of 2)

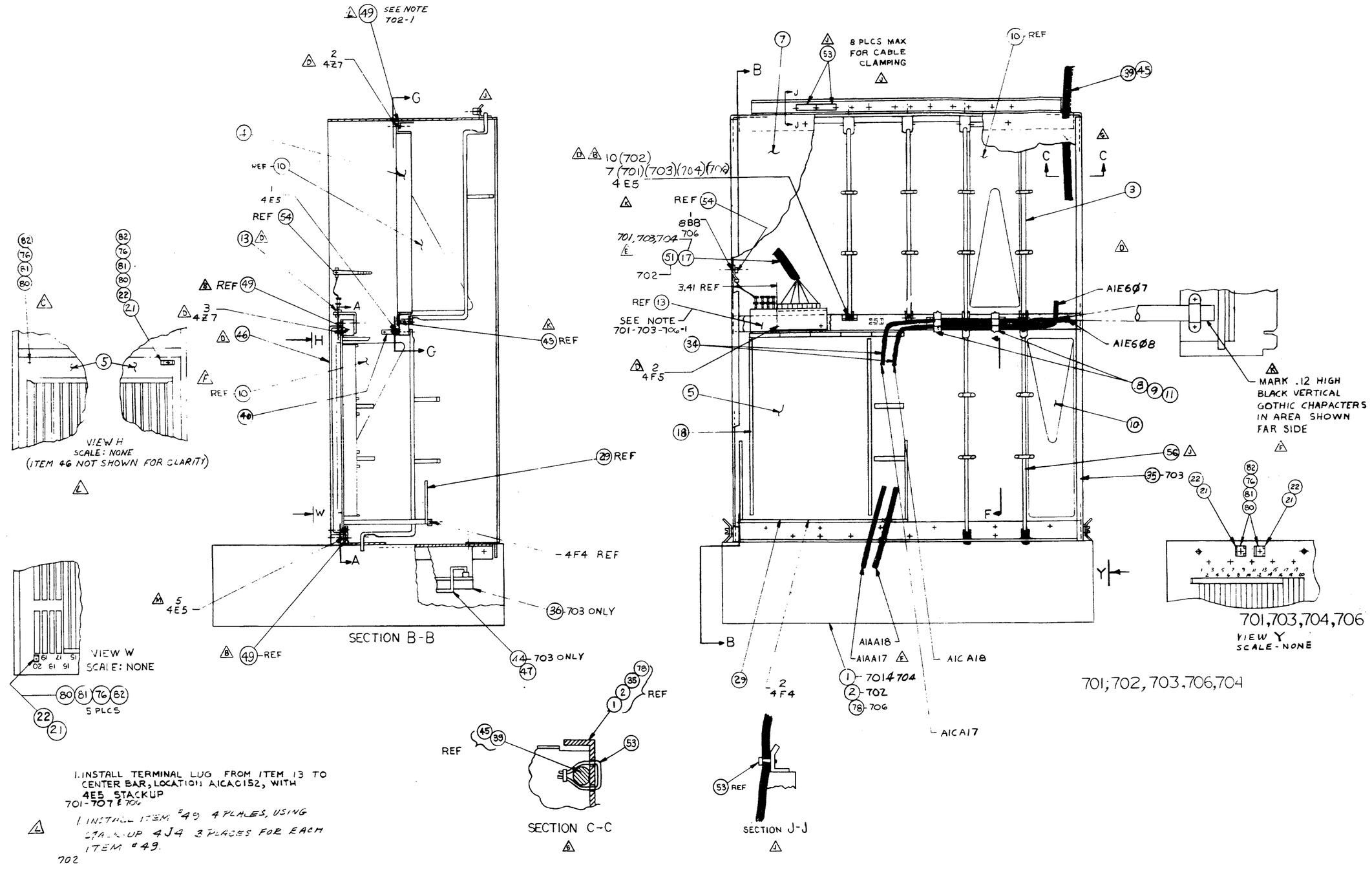
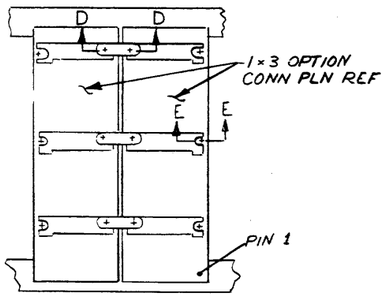
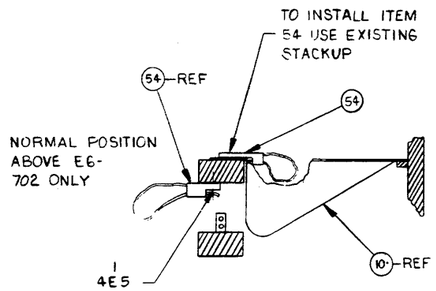


Figure 3-10-5. Logic and Option Drawer Assembly (D70030064, Rev Z, Sheet 1 of 4)

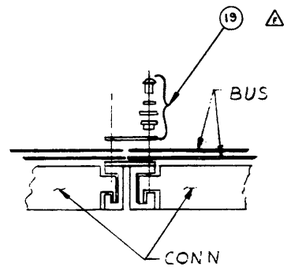


PARTIAL SECTION A-A
SCALE: NONE

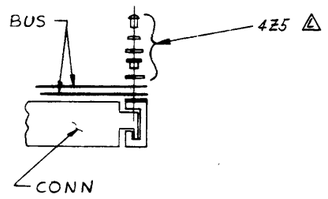
NORMAL POSITION
A4 - 701, 703, 704, 706
A1 - 702



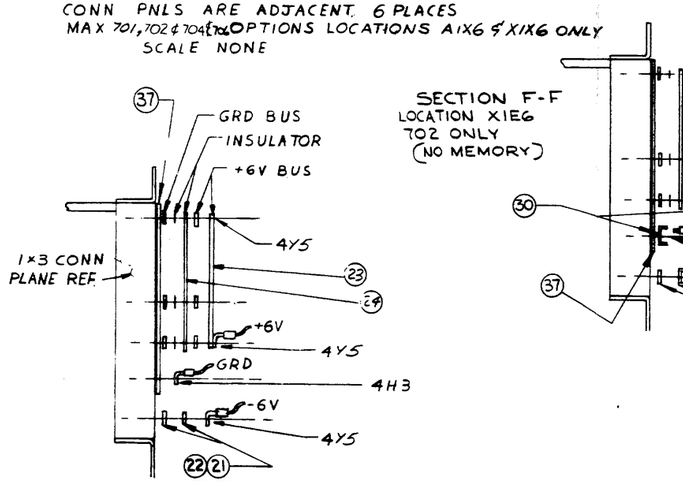
NOTE: ITEM 54 ONLY TO BE INSTALLED TO SECURE UNTERMINATED POWER WIRING IF NO OPTION (A1/A4) OR MEMORY/OPTION (E6) IS INSTALLED



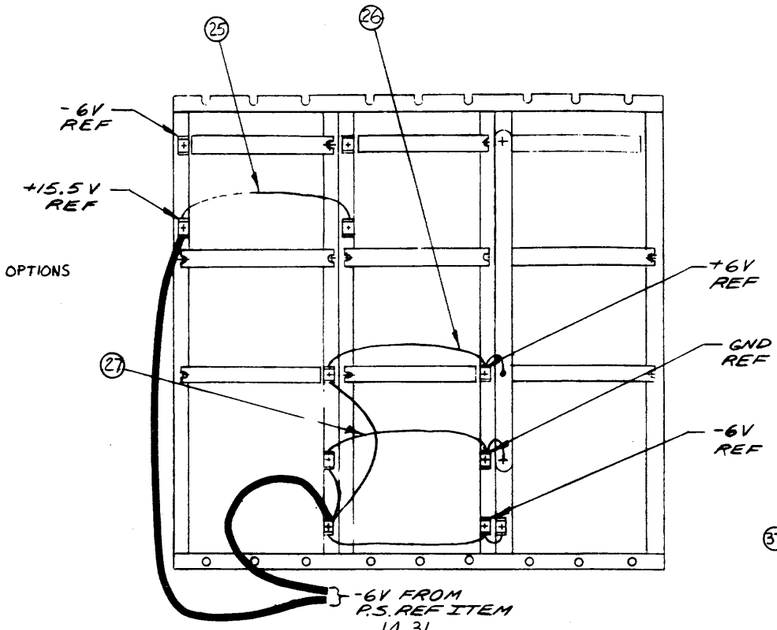
SECTION D-D
SHOWING INTERCONNECTION OF +6V & GND BUS BETWEEN ADJACENT OPTIONS
21 PLACES MAX 701 & 704 & 706
30 PLACES MAX 702
SCALE: NONE



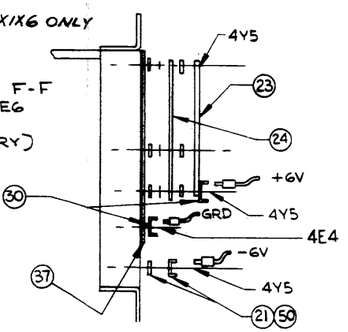
SECTION E-E
SHOWING TERMINATION OF +6V & GND BUS WHEN NO FILLER PNLS OR OPTION CONN PNLS ARE ADJACENT. 6 PLACES MAX 701, 702 & 704 & OPTIONS LOCATIONS A1X6 & X1X6 ONLY
SCALE NONE



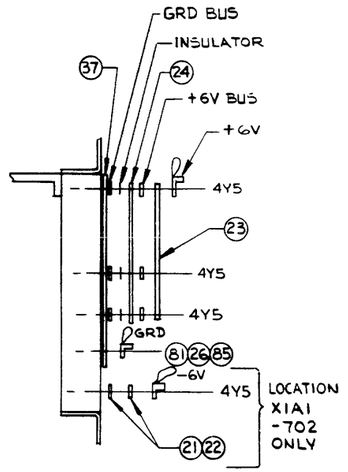
SECTION F-F
SHOWING INSTALLATION OF VOLTAGE & GND. WIRES & ASSY OF VERTICAL 6V BUS WITH INSULATOR 2 PLCES
MAX 701 & 702 & 704 & 706 LOCATION A1EX ONLY - 701 & 702 & 706 & 704



PARTIAL SECTION G-G
SHOWING MEMORY MTG & 1 x 3 OPTION
SCALE: NONE

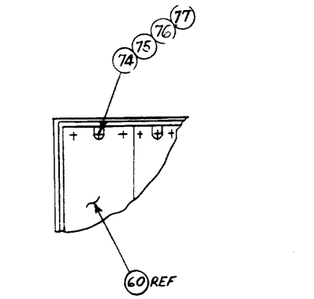


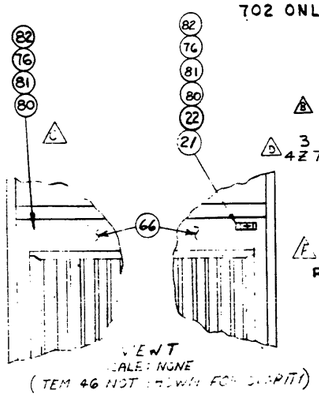
SECTION F-F
LOCATION X1E6
702 ONLY
(NO MEMORY)

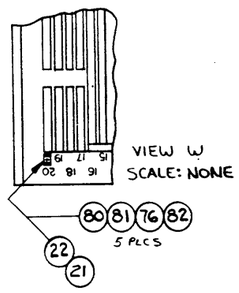


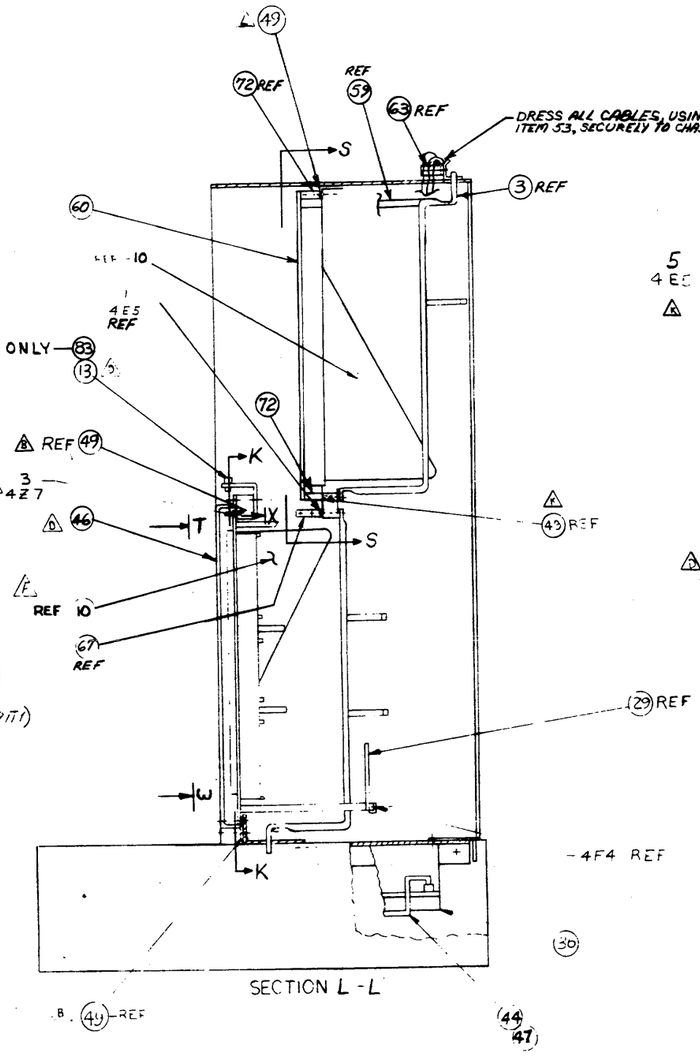
SECTION F-F
SHOWING INSTALLATION OF VOLTAGE & GND WIRES & ASSY OF VERTICAL 6V BUS WITH INSULATOR
LOCATION A1A4 - 701, 703 - 706, X1A1 - 702
SCALE: NONE

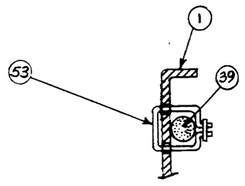
Figure 3-10-5. Logic and Option Drawer Assembly (D70030064, Rev Z, Sheet 2 of 4)

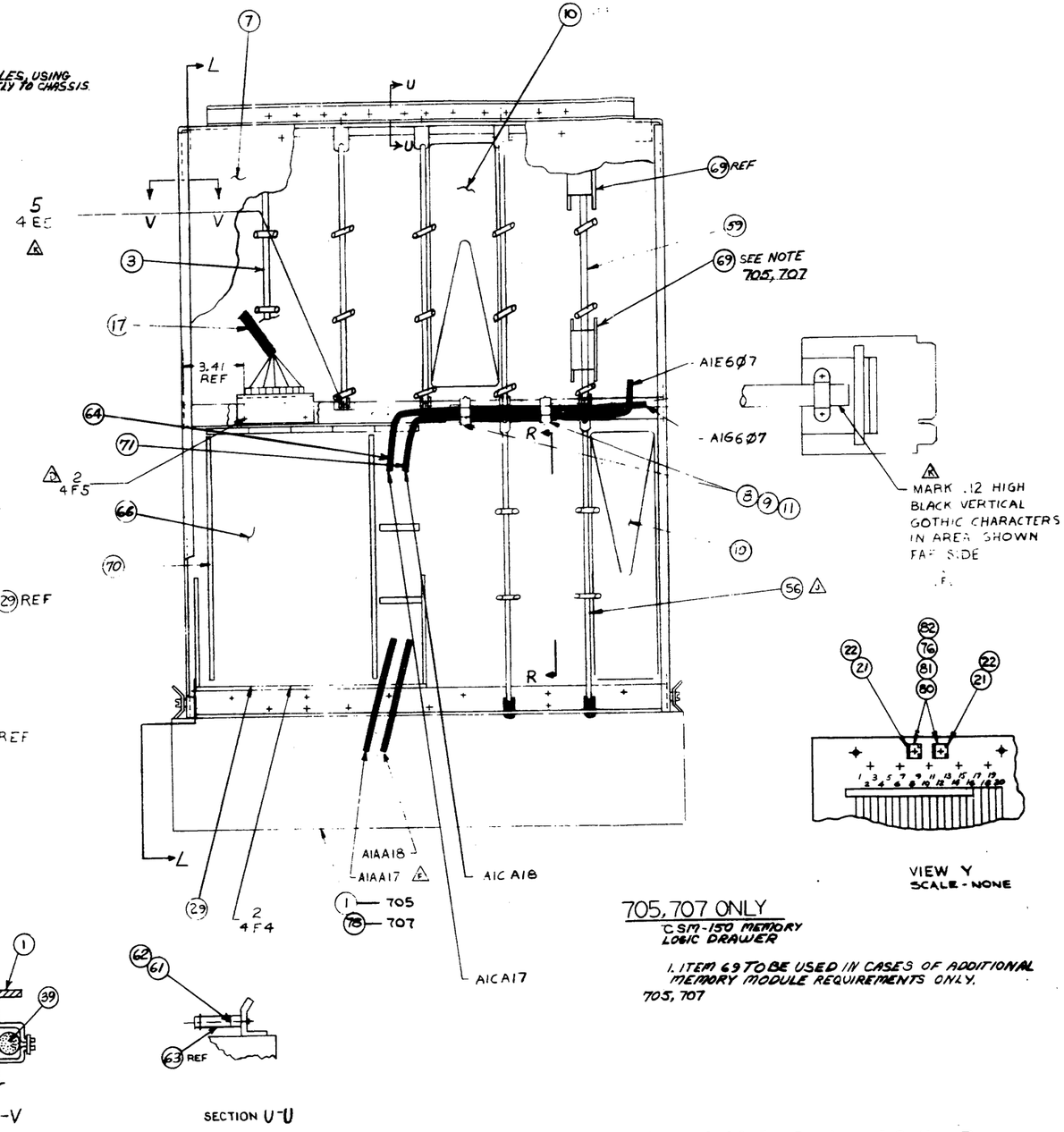








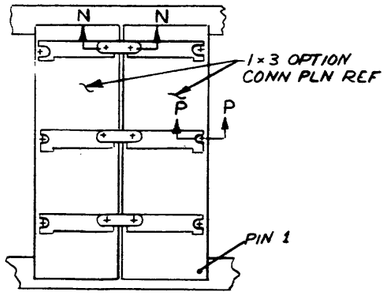




705, 707 ONLY
CSM-150 MEMORY LOGIC DRAWER

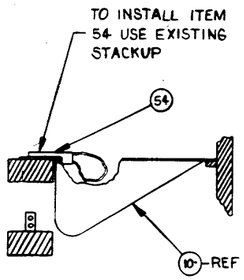
1. ITEM 69 TO BE USED IN CASES OF ADDITIONAL MEMORY MODULE REQUIREMENTS ONLY. 705, 707

Figure 3-10-5. Logic and Option Drawer Assembly (D70030064, Rev Z, Sheet 3 of 4)



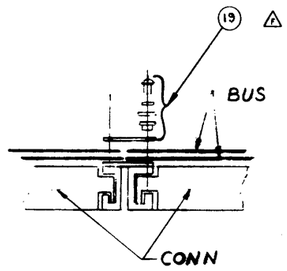
PARTIAL SECTION K-K
SCALE : NONE

NORMAL POSITION
A4 - 705, 707



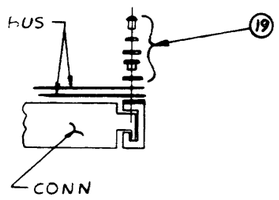
NOTE : ITEM 54 ONLY TO BE INSTALLED TO SECURE UNTERMINATED POWER WIRING IF NO OPTION (A1/A4) OR MEMORY/OPTION (E6) IS INSTALLED

△M



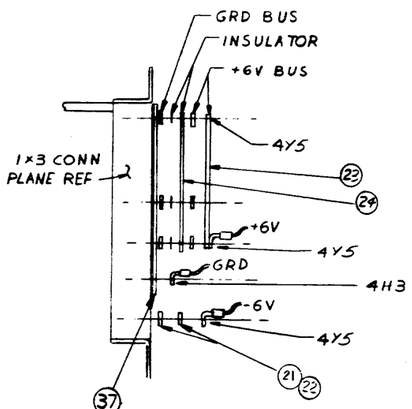
SECTION N-N
SHOWING INTERCONNECTION OF +6V & GND BUS BETWEEN ADJACENT OPTIONS
12 PLACES MAX 705, 707

SCALE : NONE

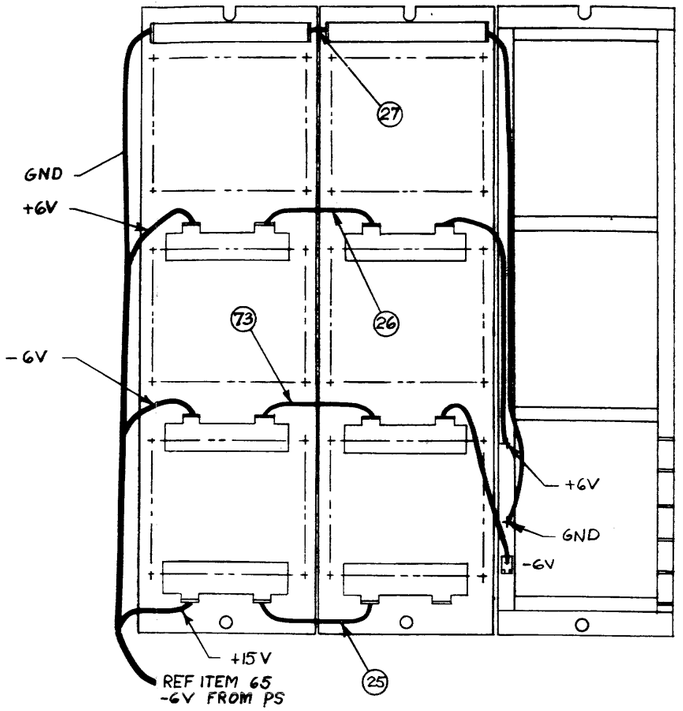


SECTION P-P
SHOWING TERMINATION OF +6V & GND BUS WHEN NO FILLER PNLS OR OPTION CONN PNLS ARE ADJACENT. 6 PLACES

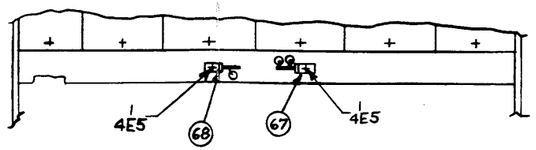
SCALE NONE



SECTION R-R
SHOWING INSTALLATION OF VOLTAGE & GND WIRES & ASSY OF VERTICAL 6V BUS WITH INSULATOR, 2 PLCS
LOCATION A1E4
SCALE : NONE

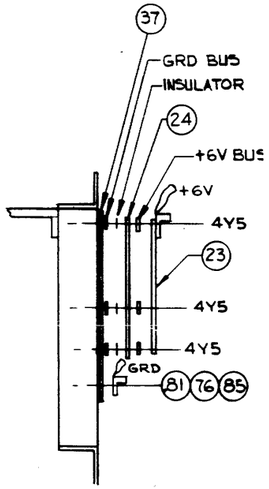


PARTIAL SECTION S-S
SHOWING MEMORY MTG & 1X3 OPTION
SCALE : FULL



VIEW X
SCALE : NONE

705, 707 ONLY
CSM-150 MEMORY LOGIC DRAWER



SECTION R-R
SHOWING INSTALLATION OF VOLTAGE & GRD WIRES & ASSY OF VERICAL 6V BUS WITH INSULATOR
LOCATION A1A4
SCALE : NONE

Figure 3-10-5. Logic and Option Drawer Assembly (D70030064, Rev Z, Sheet 4 of 4)

CHAPTER IV
MAINFRAME ILLUSTRATED PARTS BREAKDOWN

This chapter contains the illustrated parts breakdown (IPB) for the three configurations of the H316 General Purpose Computer: table top, rack-mountable, and rack-mounted, Types 316-01, 316-0100, and 316-0110, including control panel, chassis assembly, and memory. Options are documented in separate manuals.

GENERAL

The mainframe IPB is designed to aid logistical personnel in identification and procurement of replaceable parts including assemblies and components.

EQUIPMENT CODING

Coding drawings have been provided for use as an aid to further identify equipment.

METHODS OF USE

Locating a part in this chapter can be done in several ways. The method used depends upon the availability of information initially. Once having knowledge of the name of the assembly on which the part is located, find the assembly name listed in Table 4-1. Having obtained the location of the part, refer to Figures 4-1 and 4-2 in the Group Assembly Parts List and proceed as follows:

a. Identify on the illustration the equipment rack and locate the unit within the rack, indicated by a block leader line containing a number (Index).

b. Refer to the parts lists immediately following the illustration.

c. Read the information as it applies.

d. Refer to another illustration (figure) that presents a detailed breakdown of that assembly.

e. Immediately following the breakdown illustration, the parts list will contain the following information:

   1. Figure and Index Number: Each illustration is identified by a figure number. Each illustration contains leader lines and index numbers that key the order in which the parts are identified in the parts list. The only exceptions are the PACs, which are keyed in a different manner.

2. Designation: Honeywell coding designation (refer to coding explanation and coding drawings).

3. Honeywell Part Number: Honeywell part numbers are given unless otherwise indicated by an asterisk.

4. Indenture: The relationship of an item to its next higher assembly (NHA) is indicated in this column. The "B" level is an inherent part of the first preceding "A" level. The "C" level is an inherent part of the first preceding "B" level, etc.

5. Description: This column may contain the following:

   (a) Data sufficient to identify parts for ordering purposes.

   (b) Instructions for locating a more detailed illustration for breakdown, i.e., "(See Figure 4-6 for breakdown)."

   (c) Re-establishing how that particular figure was arrived at, i.e., "(Refer to Figure 4-5-1 for NHA)."

   (d) Reference to the coding drawing for a better understanding of the coding technique used, i.e., "See Drawing Number 70023412, sheet 3 for coding drawing."

6. Quantity per Assembly: Each new figure is considered an assembly and the quantity indicated in the column is the unit quantity representing the total used common to that assembly. The appearance of "REF" indicates that the quantity was stated at its first appearance (NHA).

PARTS PROCUREMENT GUIDE

1. When ordering from this manual, always reference the model and serial number of the computer.

2. Give the location of the assembly where the part is used.

3. State the part number with the description given in this manual.

4. Direct all inquiries to the following address:

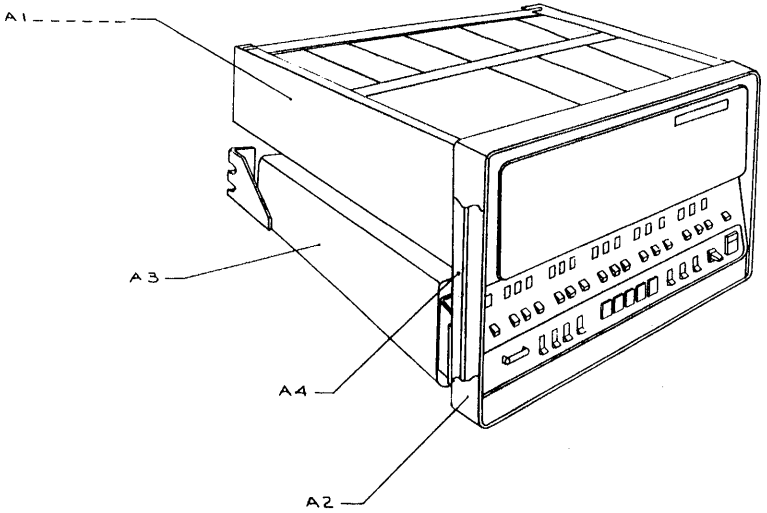
Honeywell Inc.
Old Connecticut Path
Framingham, Massachusetts 01701

Telephone: 617-879-2600
TWX: 710-380-6706

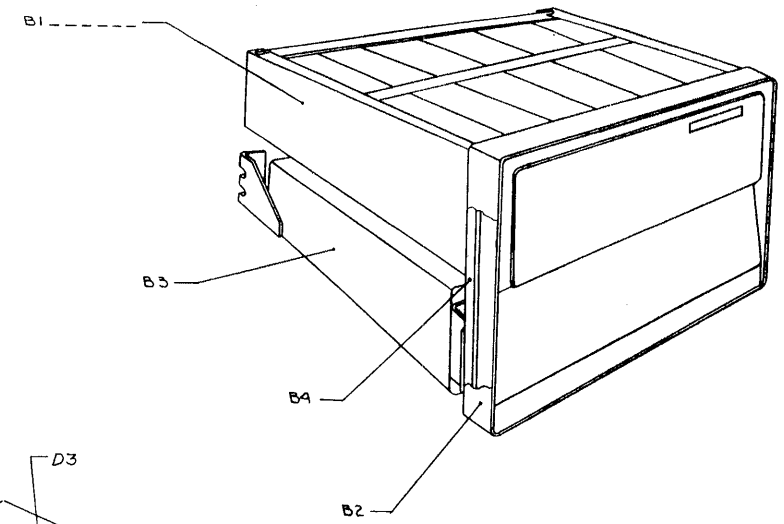
Important:

The illustrations shown are representative of all Honeywell Inc. H316 computers; therefore, the illustrations used may not show minor differences between industrial machines. If the differences are major, changes will be added to the illustration.

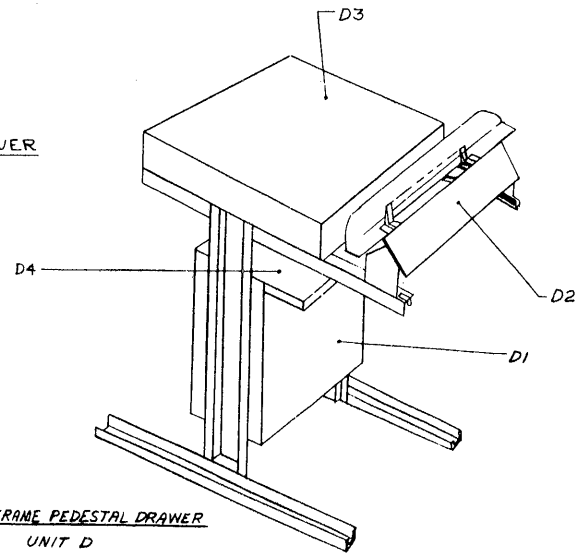
As changes are made to the equipment, this publication will be updated.



MAIN FRAME DRAWER
UNIT A

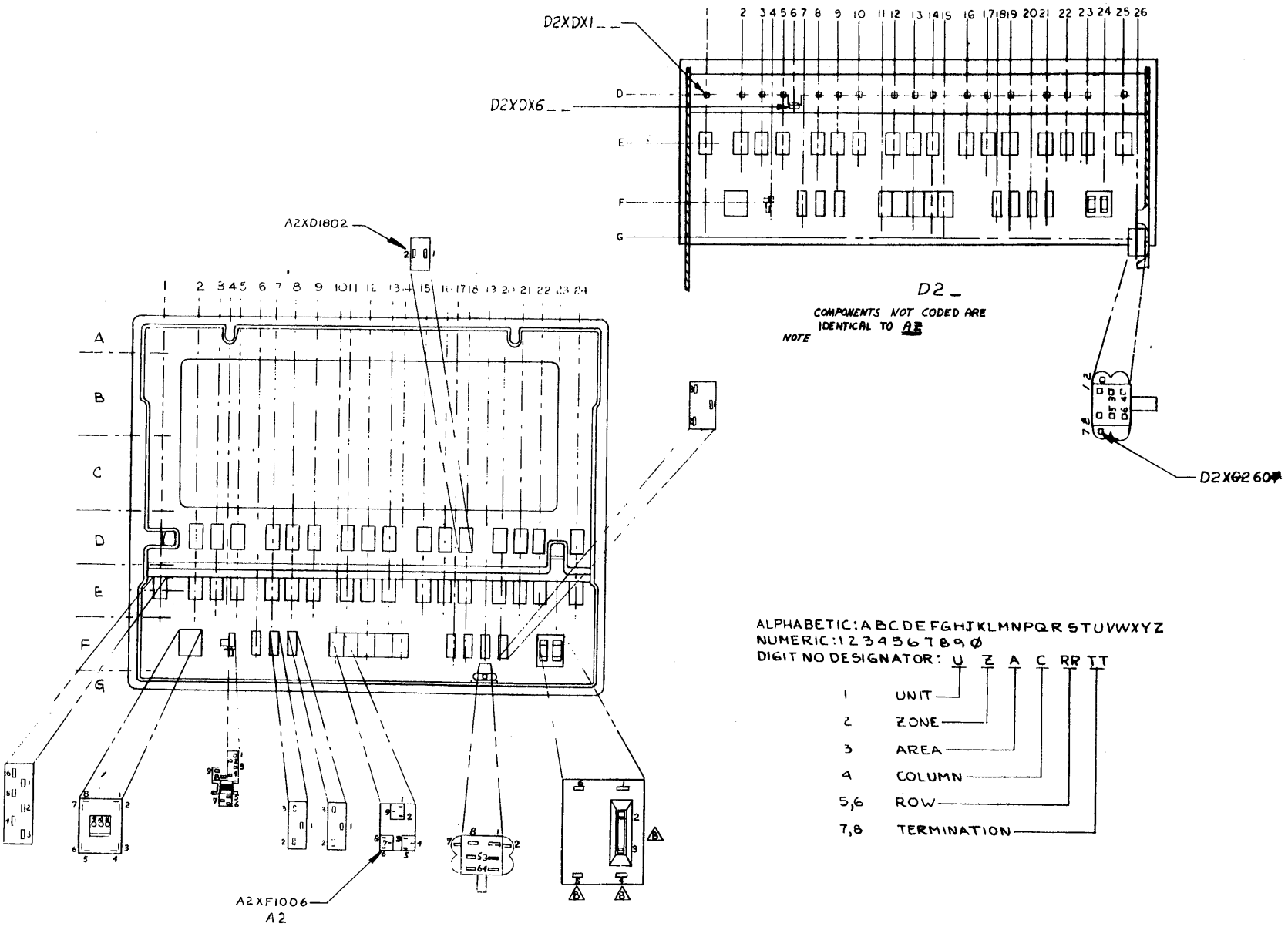


OPTION DRAWERS
UNIT B
UNIT C

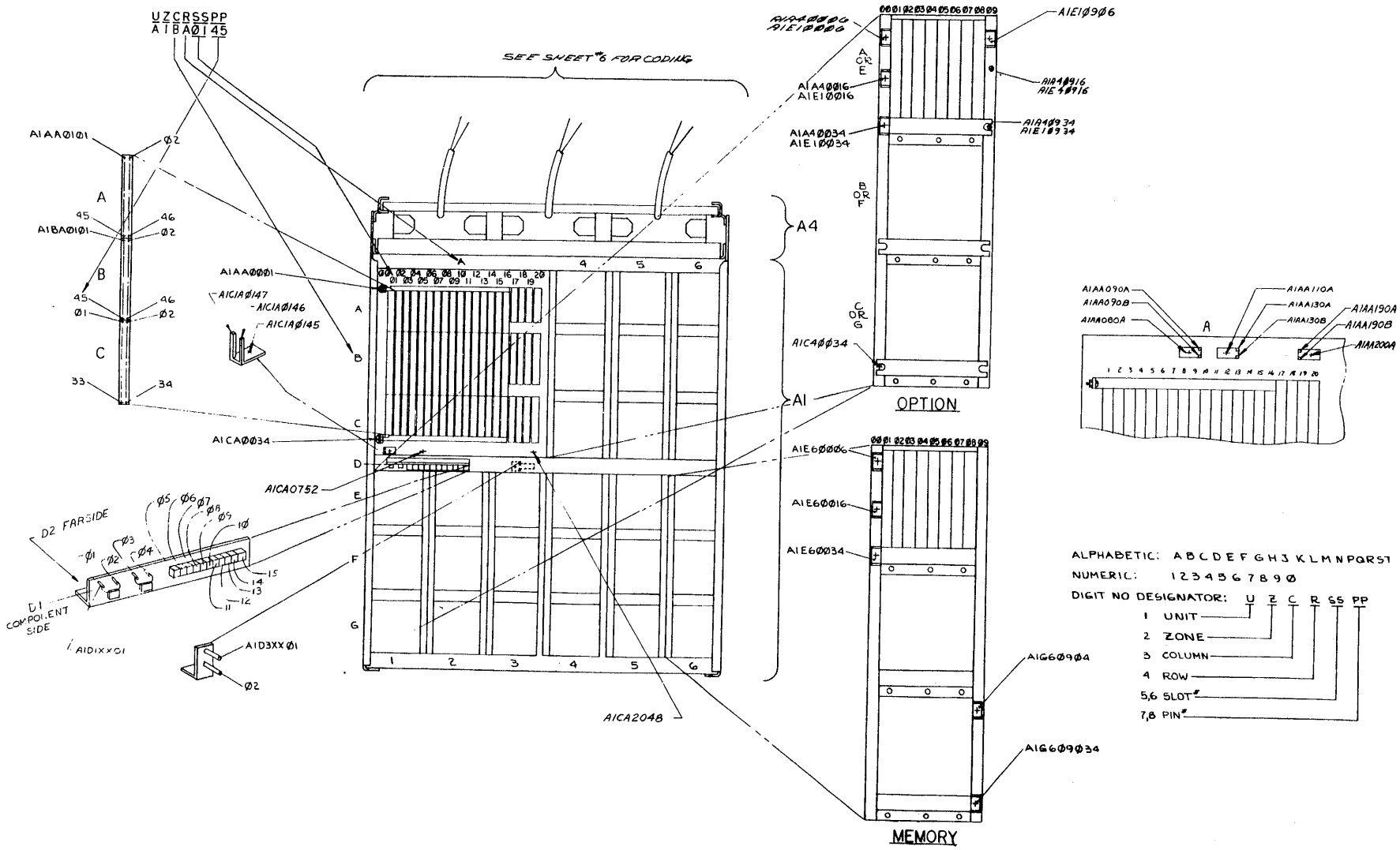


MAIN FRAME PEDESTAL DRAWER
UNIT D

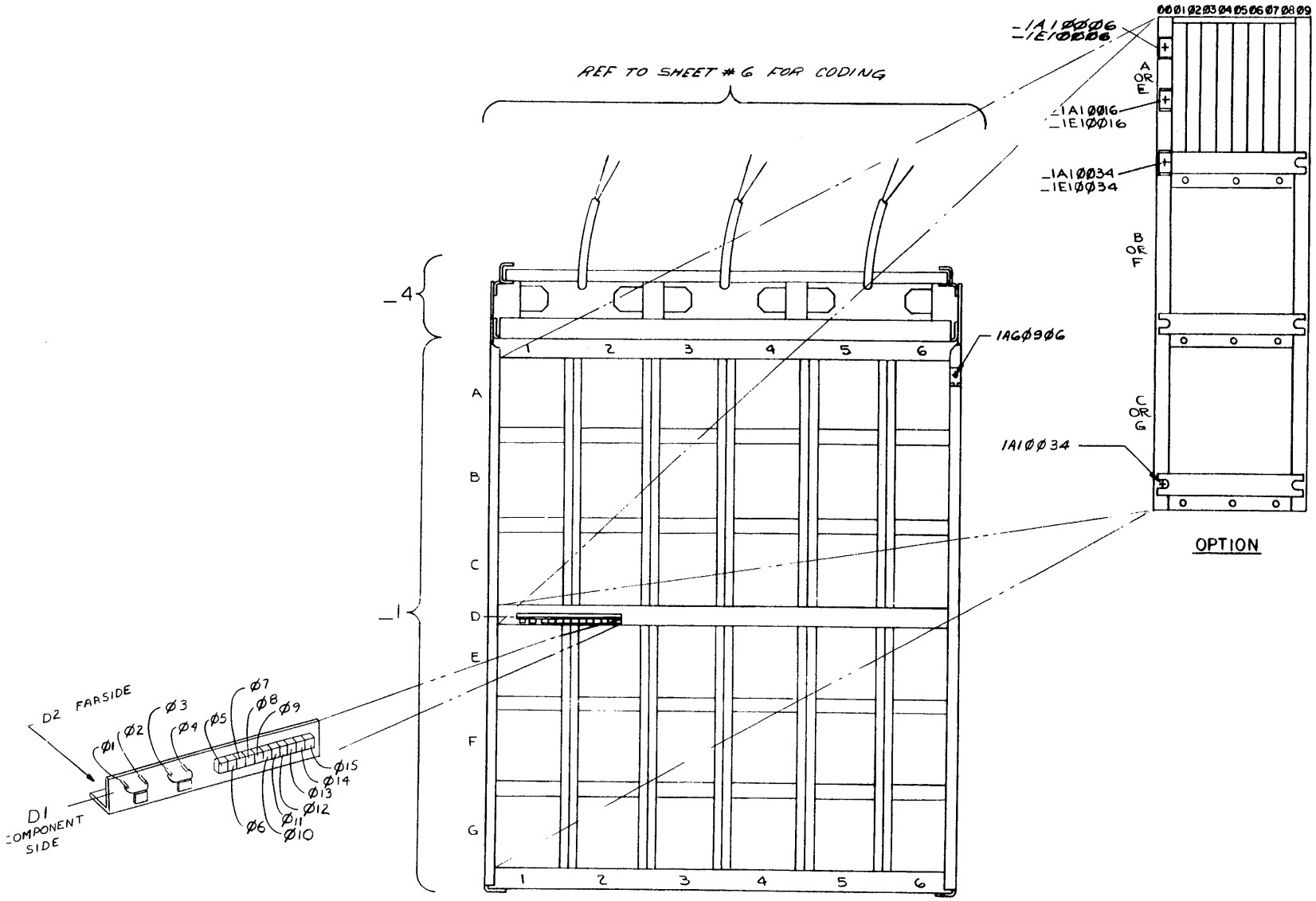
Coding Drawing No. 70023412, Rev P (Sheet 1 of 9)



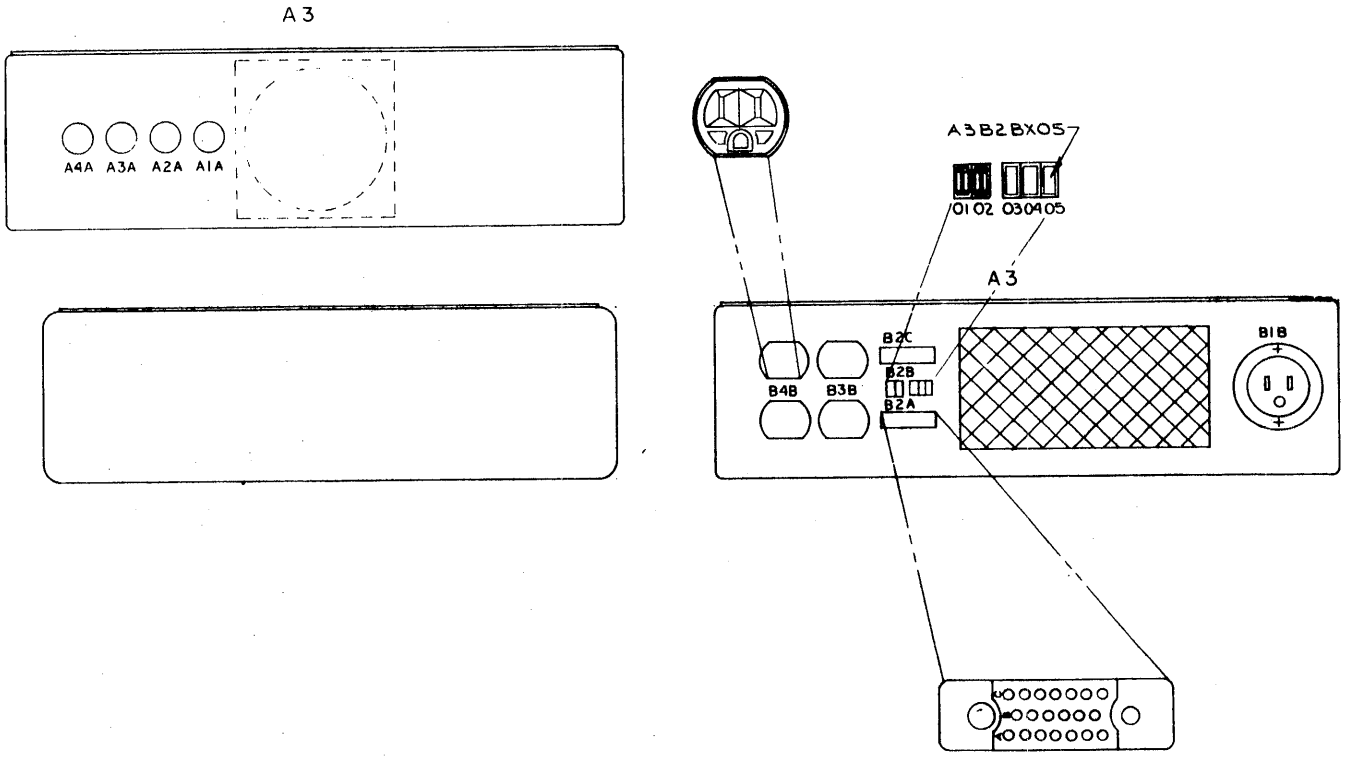
Coding Drawing No. 70023412, Rev P (Sheet 2 of 9)



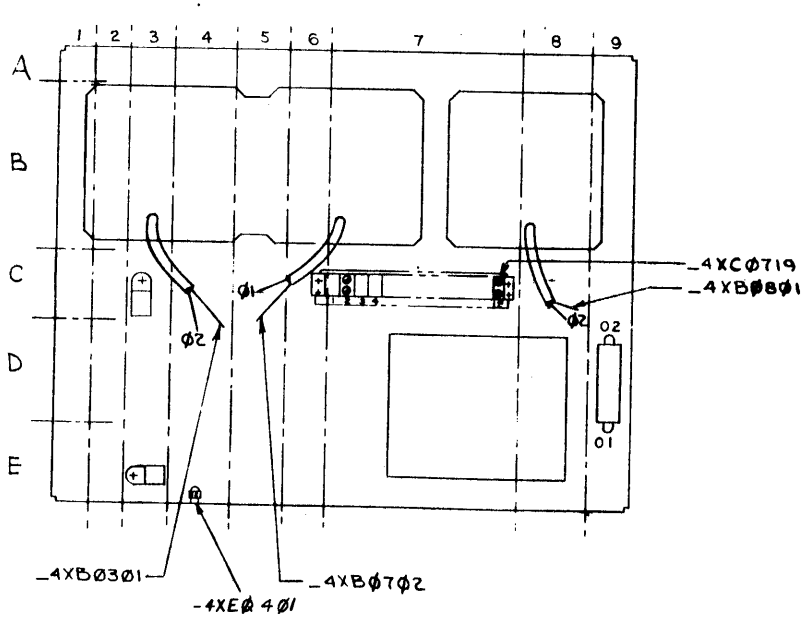
Coding Drawing No. 70023412, Rev P (Sheet 3 of 9)

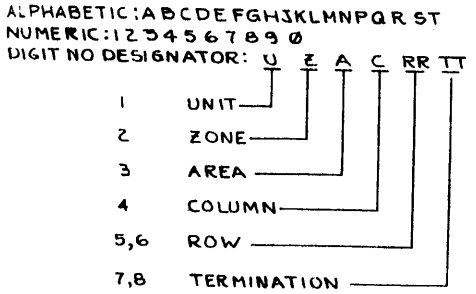


Coding Drawing No. 70023412, Rev P (Sheet 4 of 9)

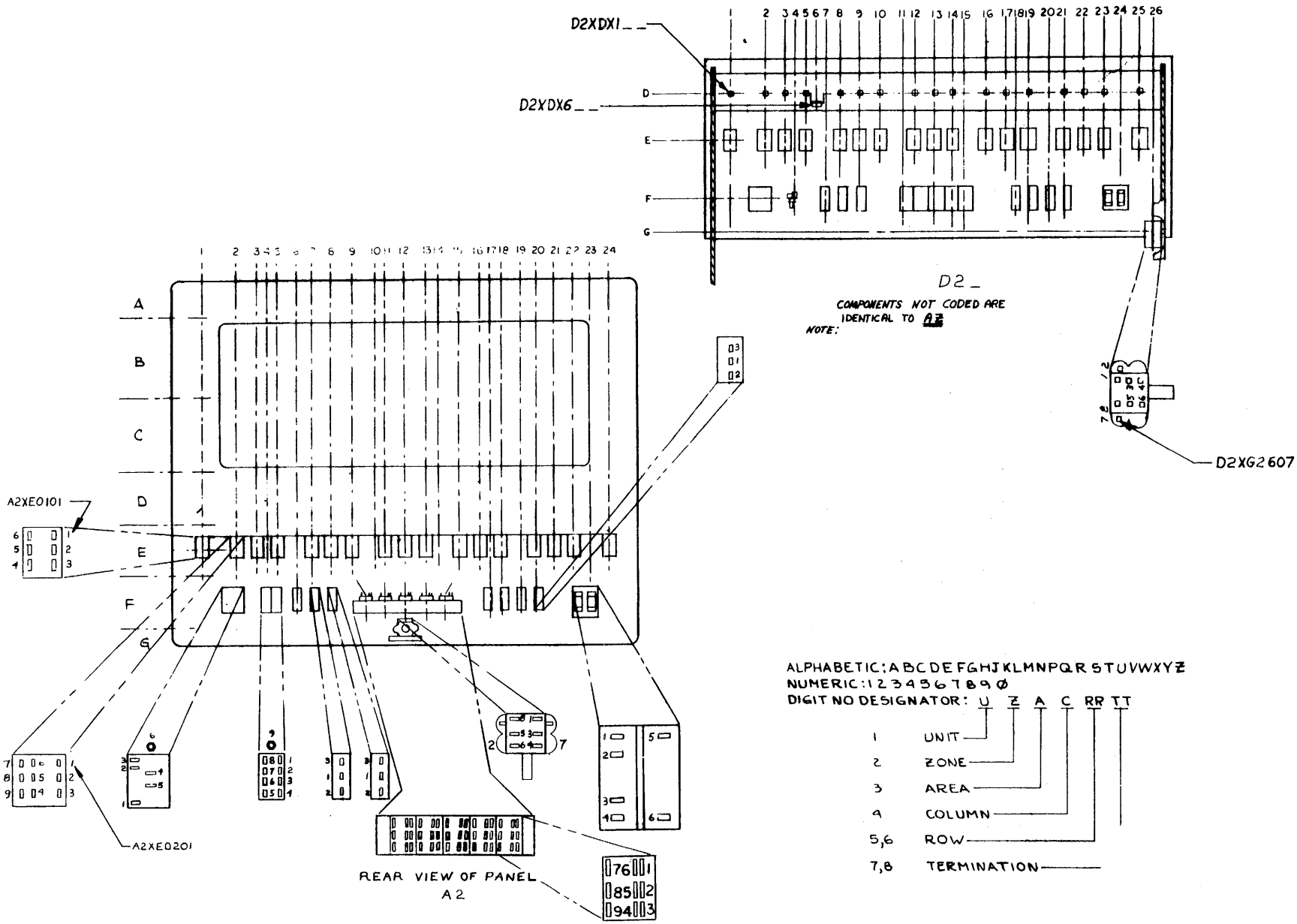


Coding Drawing No. 70023412, Rev P (Sheet 5 of 9)

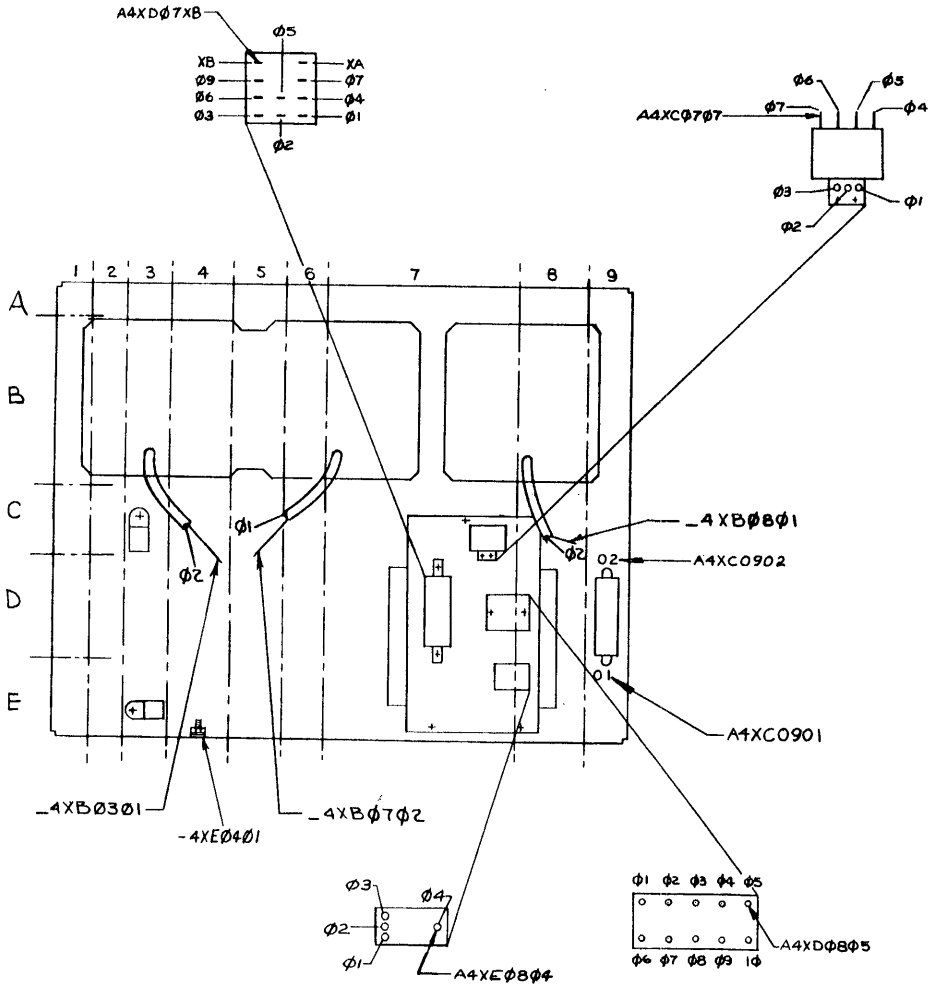




Coding Drawing No. 70023412, Rev P (Sheet 6 of 9)



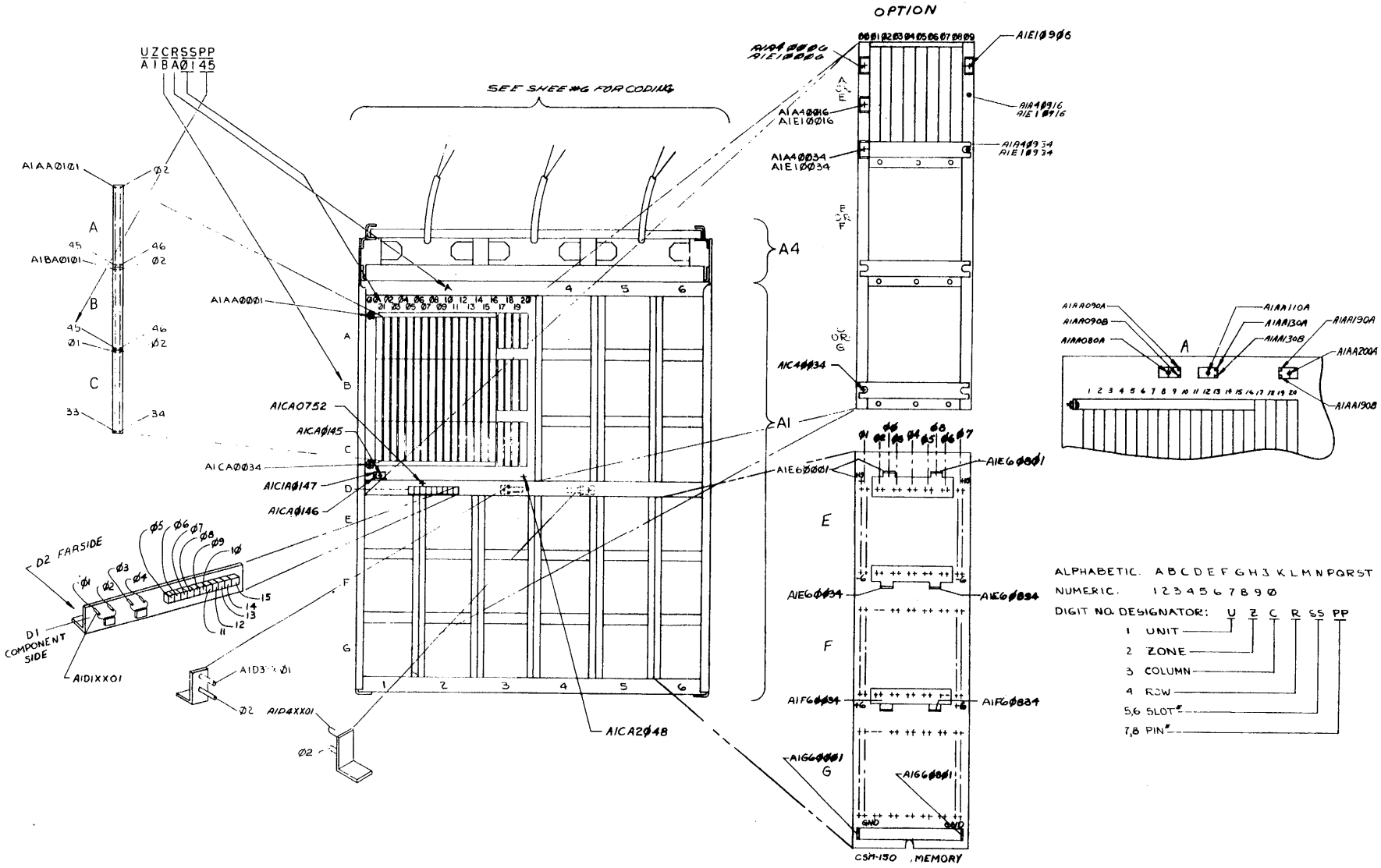
Coding Drawing No. 70023412, Rev P (Sheet 7 of 9)



ALPHABETIC: A B C D E F G H J K L M N P Q R S T
NUMERIC: 1 2 3 4 5 6 7 8 9 Ø
DIGIT NO DESIGNATOR: U Z A C RR TT

1	UNIT
2	ZONE
3	AREA
4	COLUMN
5,6	ROW
7,8	TERMINATION

Coding Drawing No. 70023412, Rev P (Sheet 8 of 9)



Coding Drawing No. 70023412, Rev P (Sheet 9 of 9)

GROUP ASSEMBLY PARTS LIST

Table 4-1 lists the figure number used to locate the Group Assembly Parts List for a particular subassembly

Table 4-1
Figure Number Cross Reference

Fig. No.	Description	Part No.
4-1	H316 General Purpose Computer, Rack-Mounted Model, Type 316-01	70023278501
4-2	H316 General Purpose Computer, Rack-Mounted Model, Types 316-0100 and 316-0110	70030063701
4-3	H316 General Purpose Computer, Table Top Model, Type 316-01	70023278703
4-4	H316 General Purpose Computer, Table Top Model, Types 316-0100 and 316-0110	70030071703
4-5	Control Panel, Type 316-01	70023065
4-6	Control Panel, Types 316-0100 and 316-0110	70030065
4-7	Chassis Assembly, Type 316-01	70023235
4-8	Chassis Assembly, Types 316-0100 and 316-0110	70030054701
4-9	Mainframe Logic and Option Drawer Assembly, Type 316-01	70023232
4-10	Mainframe Logic and Option Drawer Assembly, Types 316-0100 and 316-0110	70030064701
4-11	CSM-160 Core Memory Unit, Types 316-01, 316-0100, and 316-0110	70023577
4-12	CSM-150 Core Memory Unit, Types 316-01, 316-0100, and 316-0110	70032935
4-13	Logic Module Layout, Types 316-01, 316-0100, and 316-0110	No number
4-14	Cable Block Diagram	No number
4-15	Cable Assembly, Power, Electrical, Type 316-01	70023838701
4-16	Cable Assembly, Power, Electrical, Types 316-0100 and 316-0110	70030072701
4-17	Cable Assembly, Power, Electrical, Types 316-01, 316-0100, and 316-0110	70023837701
4-18	Cable Assembly, Special Purpose, Type 316-01	70024016701
4-19	Cable Assembly, Special Purpose, Types 316-0100 and 316-0110	70029942701
4-20	Cable Assembly, Special Purpose, Type 316-01	70024010701
4-21	Cable Assembly, Special Purpose, Types 316-0100 and 316-0110	70029943701
4-22	Cable Assembly, Special Purpose, μ-PAC to μ-PAC, Types 316-01, 316-0100, and 316-0110	70013826701

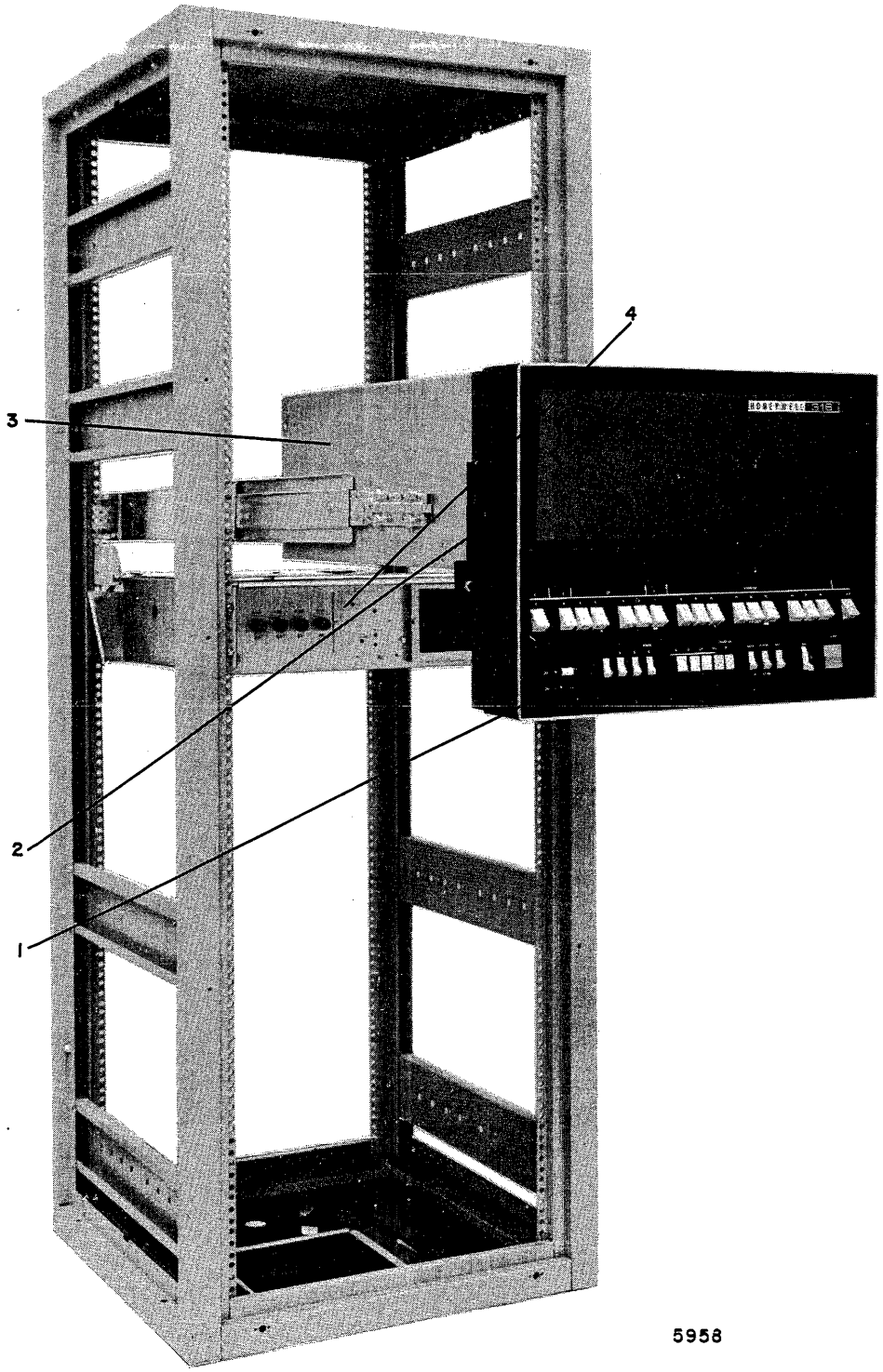


Figure 4-1. H316 General Purpose Computer, Rack-Mounted Model, Type 316-01

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-1-	A	70023278701	A	H316 GENERAL PURPOSE COMPUTER, RACK-MOUNTED MODEL, TYPE 316-01.	
-1	A2	70023065	B	CONTROL PANEL ASSEMBLY (see Figure 4-5 for breakdown and Coding Drawing No. 70023412, Sheet 2).	1
-2	A4	70023235	B	CHASSIS ASSEMBLY (see Figure 4-7 for breakdown and Coding Drawing No. 70023412, Sheet 6).	1
-3	A1	70023232	B	MAINFRAME LOGIC AND MEMORY DRAWER (see Figure 4-9 for breakdown and Coding Drawing No. 70023412, Sheet 3).	1
-4	A3	70960061001	B	POWER SUPPLY (see Coding Drawing No. 70023412, Sheet 5).	

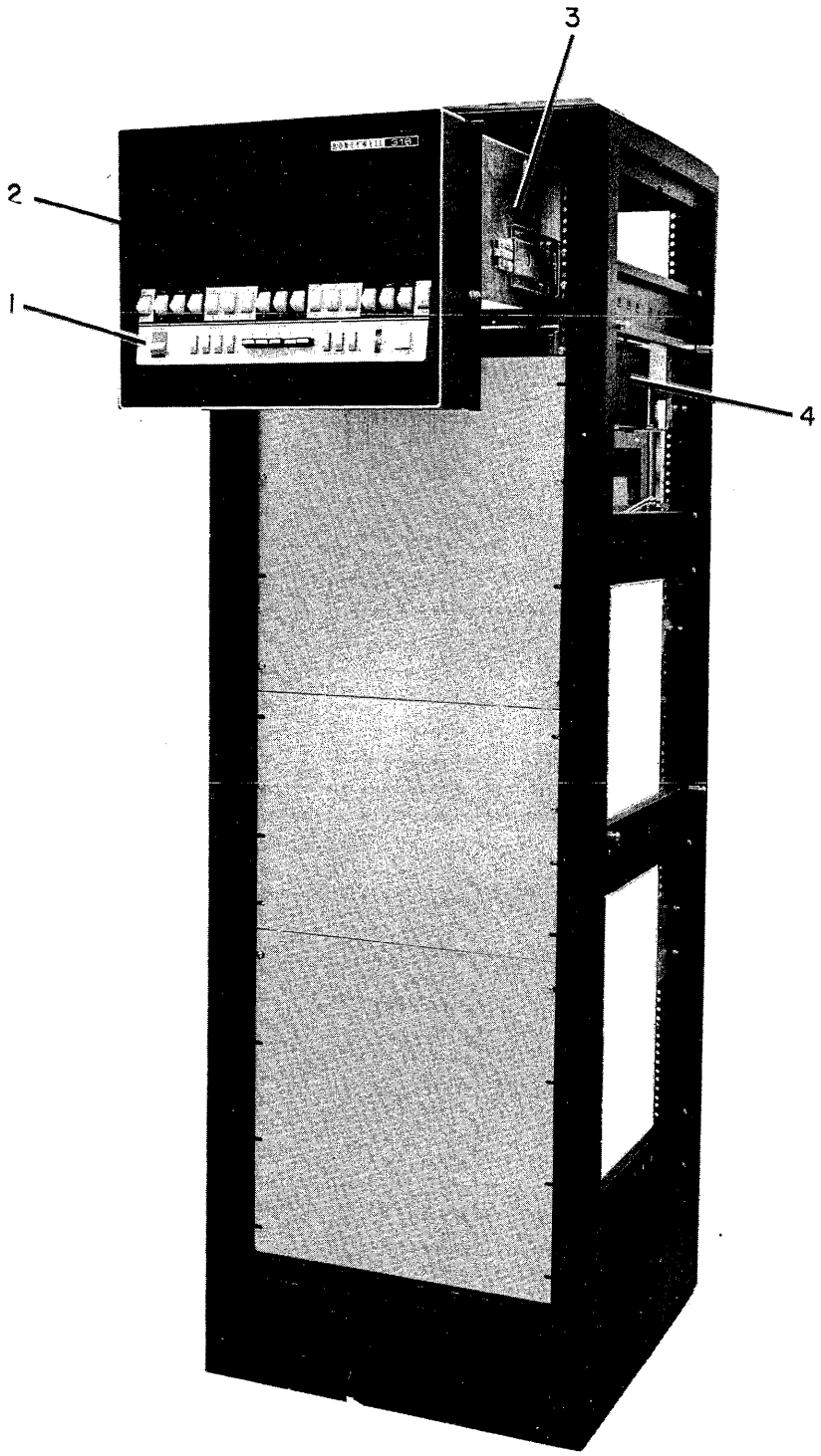


Figure 4-2. H316 General Purpose Computer, Rack-Mounted Model, Types 316-0100 and 316-0110

Fig. & Index No.	Designation	Part No.	Indenture	Description	Qty per Ass'y
4-2-	A	70030063701	A	H316 GENERAL PURPOSE COMPUTER, RACK-MOUNTED MODEL, TYPES 316-0100 and 316-0110.	
-1	A2	70030065	B	CONTROL PANEL ASSEMBLY (see Figure 4-6 for breakdown and Coding Drawing No. 70023412, Sheet 7).	1
-2	A4	70030054	B	CHASSIS ASSEMBLY (see Figure 4-8 for breakdown and Coding Drawing No. 70023412, Sheet 8).	1
-3	A1	70030064701	B	MAINFRAME LOGIC AND MEMORY DRAWER (see Figure 4-10 for breakdown and Coding Drawing No. 70023412, Sheet 3).	1
-4	A3	70023699	B	POWER SUPPLY (see Coding Drawing No. 70023412, Sheet 5).	1

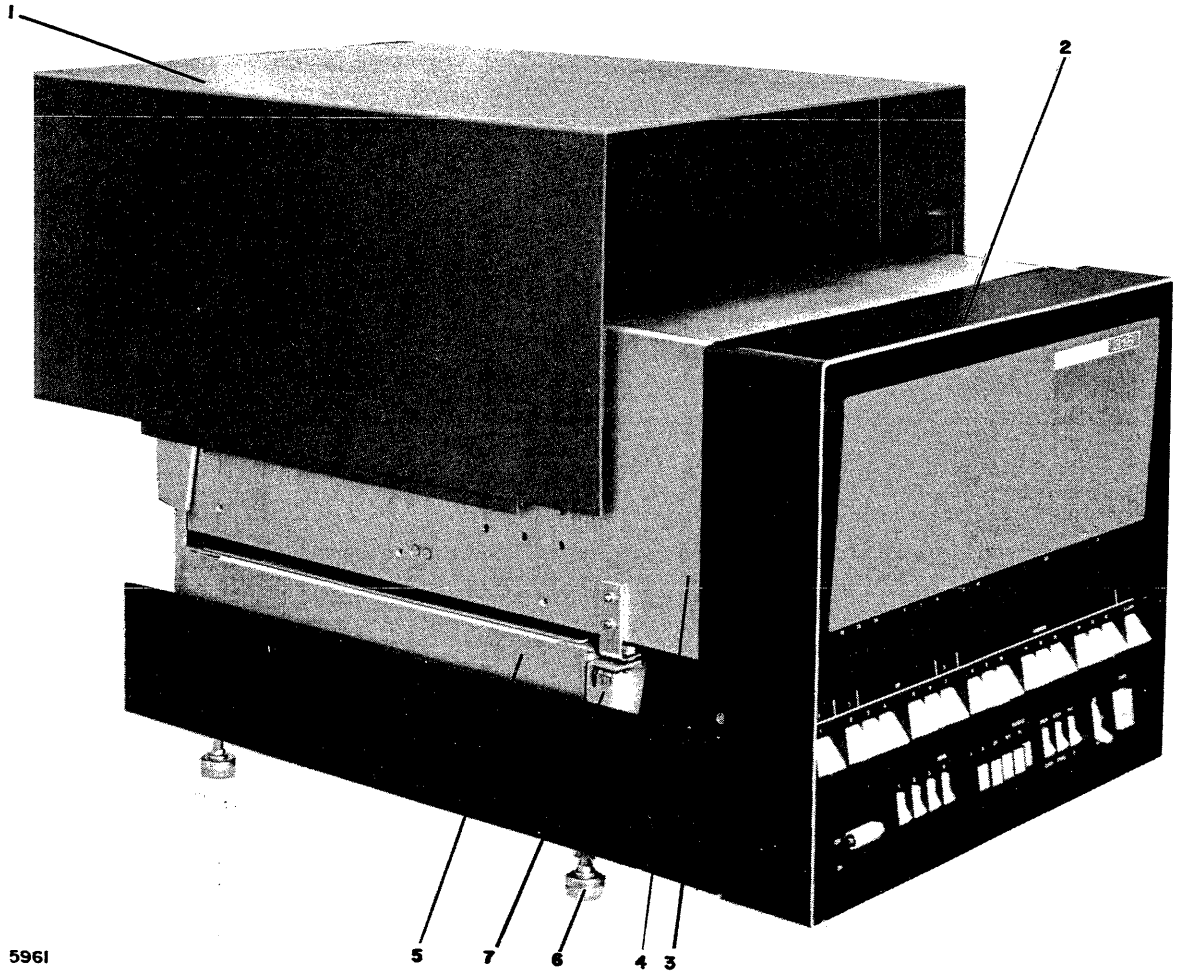


Figure 4-3. H316 General Purpose Computer,
Table Top Model, Type 316-01

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-3-	A	70023278703	A	H316 GENERAL PURPOSE COMPUTER, TABLE TOP MODEL, TYPE 316-01.	
-1		70023697701	B	COVER TOP.	1
-2	A2	70023065	B	CONTROL PANEL ASSEMBLY (same as Rack-Mounted Model, see Figure 4-5 for breakdown).	1
-3	A4	70023235701	B	CHASSIS ASSEMBLY (same as Rack-Mounted Model, see Figure 4-7 for breakdown).	1
-4	A1	70023232701	B	MAINFRAME LOGIC AND MEMORY DRAWER (same as Rack-Mounted Model; see Figure 4-9 for breakdown).	1
-5	A3	70023699701	B	POWER SUPPLY, MODIFIED (same as Rack Mounted Model except for mount-ing hardware).	1
-6		912251001	C	LEVELING FOOT.	4
-7		906320002	C	SNAPSLIDE FASTENER.	2

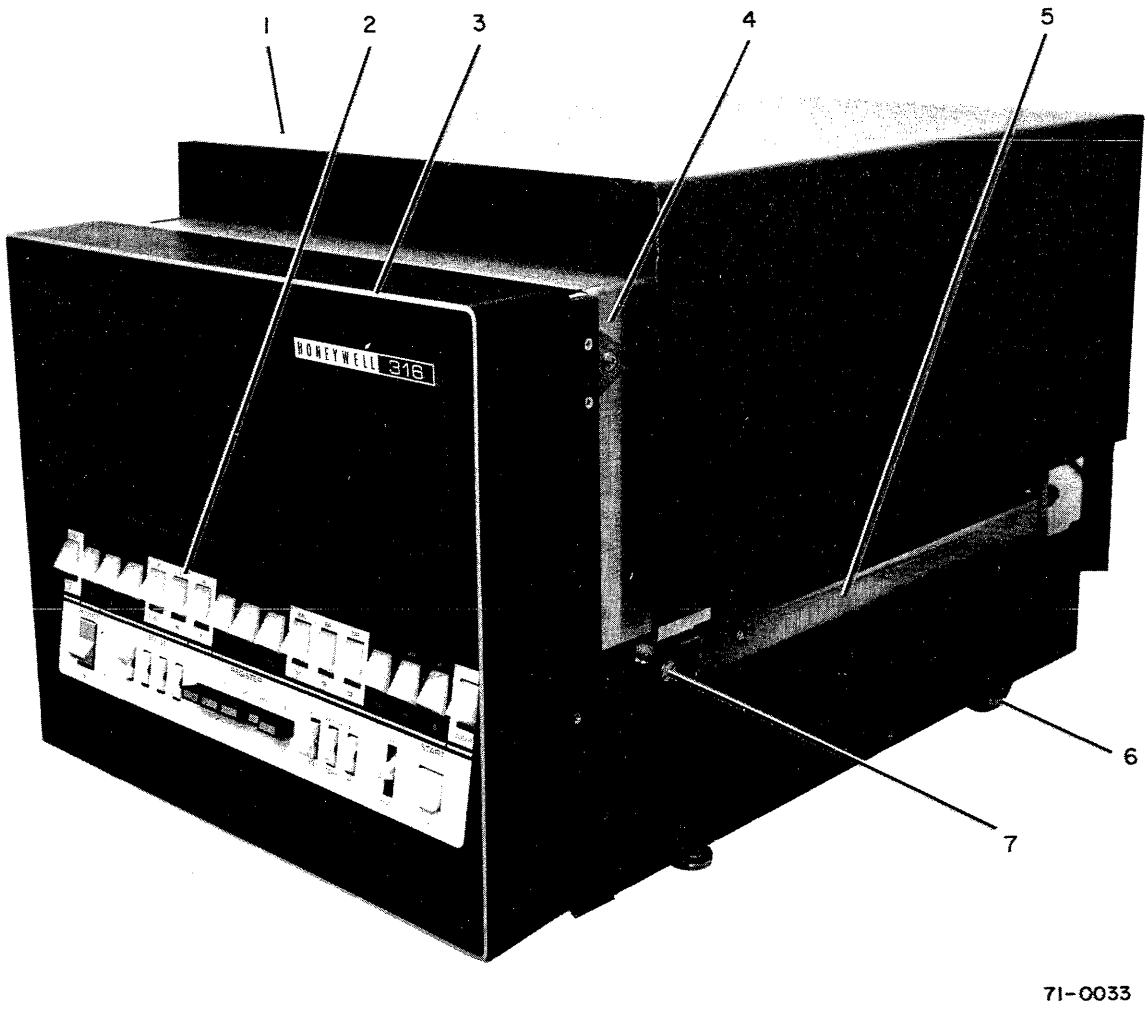


Figure 4-4 H316 General Purpose Computer, Table Top Model, Types 316-0100 and 316-0110

Fig. & Index No.	Designation	Part No.	Indenture	Description	Qty per Ass'y
4-4-	A	70030071703	A	H316 GENERAL PURPOSE COMPUTER, TABLE TOP MODEL, TYPES 316-0100 and 316-0110.	
-1		70023697701	B	COVER TOP.	1
-2	A2	70030065	B	CONTROL PANEL ASSEMBLY (same as Rack-Mounted Model, see Figure 4-6 for breakdown).	1
-3	A4	70030054701	B	CHASSIS ASSEMBLY (same as Rack-Mounted Model, see Figure 4-8 for breakdown).	1
-4	A1	70030064	B	MAINFRAME LOGIC AND MEMORY DRAWER (same as Rack-Mounted Model, see Figure 4-10 for breakdown).	1
-5	A3	70023699701	B	POWER SUPPLY, MODIFIED (same as Rack-Mounted Model except for mounting hardware).	1
-6		912251001	C	LEVELING FOOT.	4
-7		906320002	C	SNAPSLIDE FASTENER.	2

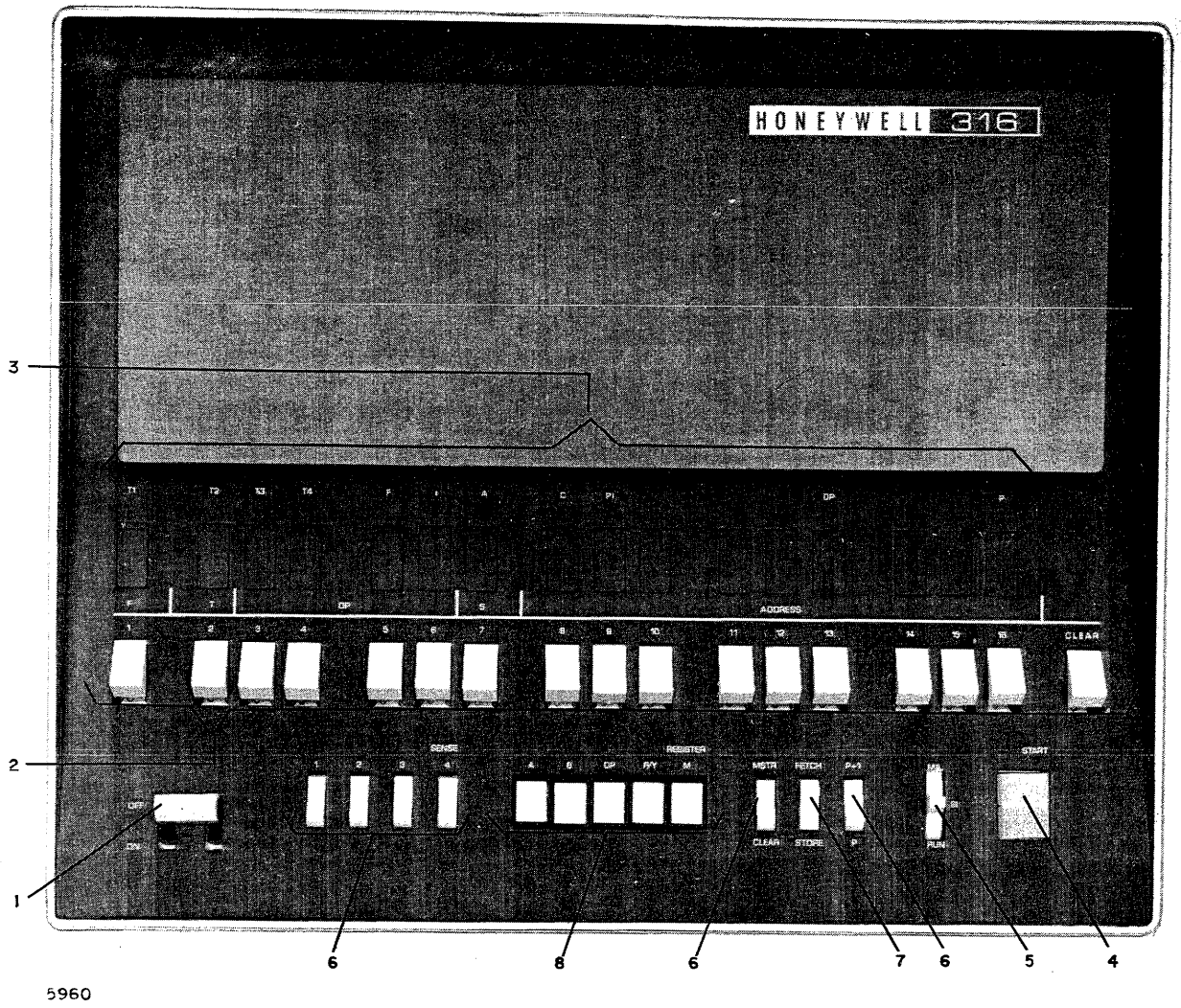


Figure 4-5. Control Panel, Type 316-01

Fig. & Index No.	Designation	Part No.	Indenture	Description	Qty per Ass'y
4-5-	A2	70023065	B	CONTROL PANEL ASSEMBLY (Refer to Figure 4-1-1 and 4-3-1, Type 316-01 for NHA)	Ref.
-1	A2E23	70960056001	C	CIRCUIT BREAKER, DOUBLE POLE: 1st pole series trip at 30A, 250 Vac 50/60 Hz, curve 3; 2nd pole relay trip 6 Vdc, 50 mA curve p.	1
-2	A2E24, 22, 21, 20, 18, 16, 15, 13, 12, 11, 09, 08, 07, 05, 03, 02, 01	70934278001	C	SWITCH PUSH-ROCKER DPDT: 60A ac; 0.5A dc.	17
		70023068701	C	BUTTON, CAP-MOLDED LIGHT: grey plastic; 0.527 by 0.912 inch.	17
-3	A2D24, 22, 21, 20, 18, 16, 15, 13, 12, 11, 09, 08, 07, 05, 03, 02,	70908281001	C	HOUSING, LIGHT INDICATOR.	16
		70935081203	C	LIGHT, INDICATOR: 28V at 0.04A; yellow lens.	16
-4	A2F2		C	PUSHBUTTON LIGHT INDICATOR ASSEMBLY CONSISTING OF:	1
		70935031002	D	LAMPHOLDER ASSEMBLY: short flange type	1
		70910353001	D	LENS SWITCH ACTUATOR.	1
		70934263001	D	SWITCH, PUSH - SPDT: 5A at 250V.	1
		70945002002	D	LAMP, INCANDESCENT: 0.04 A at 28V 7-1 3/4 bulb, midget flange base.	2
-5	A2F4	70934020003	C	SWITCH, LEVER LOCKING: 3 position, 3A, 200 W.	1
-6	A2F06, 08, 17, 18, 19, 20	70934276001	C	SWITCH, PUSH, ROCKER - SPDT: 6A at 125 Vac, 3A at 250 Vac; 1.0 A dc.	6
-7	A2F07	70934272001	C	SWITCH, PUSH, ROCKER - SPDT: 6A at 125 Vac; 3A at 250 Vac, 1.0 A dc.	1
-8	A2F10, 11, 12 13, 14		C	PUSHBUTTON ASSEMBLY CONSISTING OF:	1
		70934275001	D	SWITCH, PUSH, INTERLOCK: 5 station interlock; 3A, 300W max; ac noninductive load.	1
		70910303001	D	PUSHBUTTON: molded plastic, black/ white face.	5
		70943083002	D	SEMICONDUCTOR DEVICE, DIODE: silicon type.	1

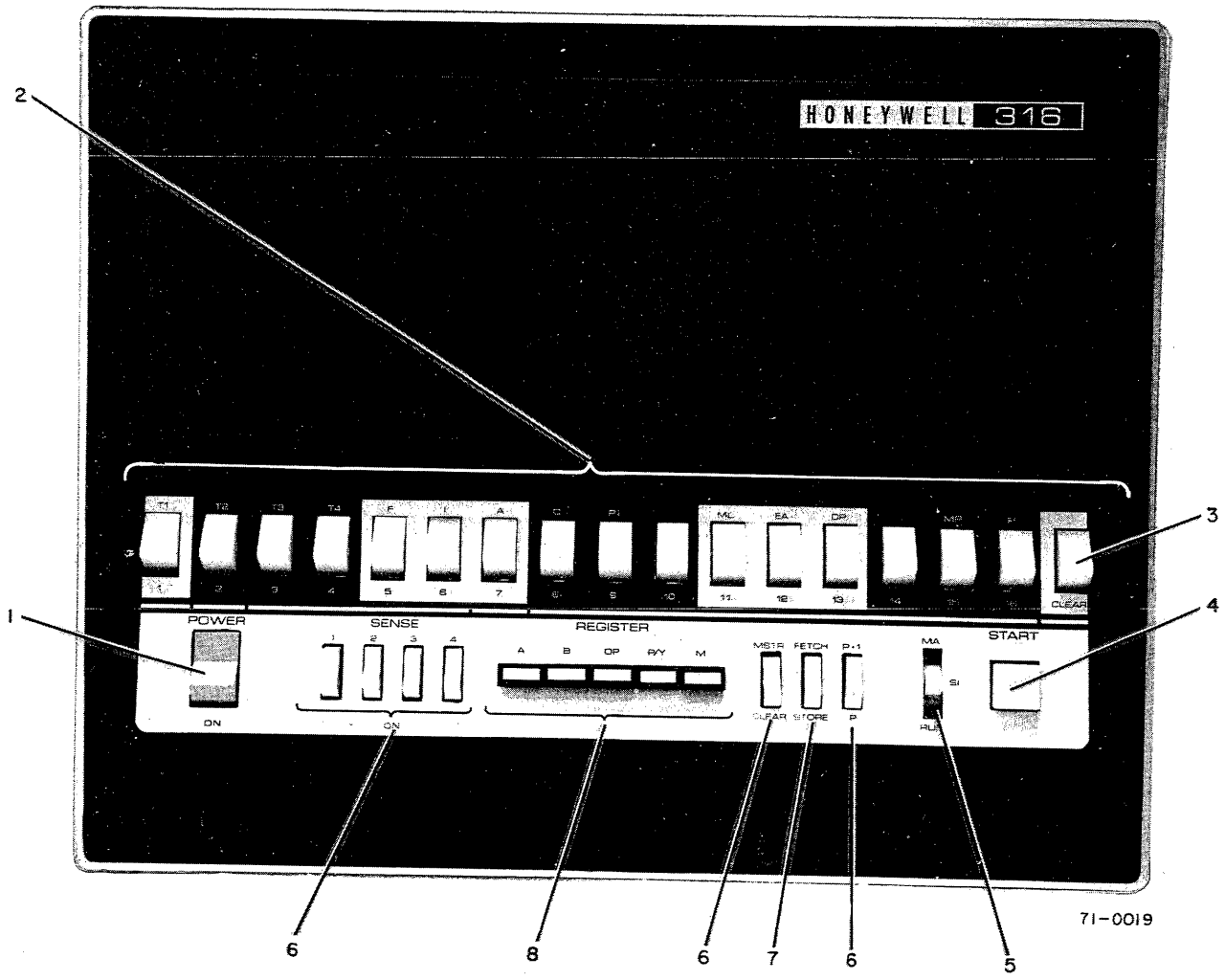


Figure 4-6. Control Panel, Types 316-0100 and 316-0110

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-6-	A2	70030065	B	CONTROL PANEL ASSEMBLY (Refer to Figures 4-2-1 and 4-4-1, Types 316-0100 and 316-0110 for NHA).	Ref.
-1	A2E23	70960058001		CIRCUIT BREAKER, DOUBLE POLE: 1st pole series trip at 30A, 250 Vac 50/60 Hz, curve 3; 2nd pole relay trip 6 Vdc, 50 mA curve p.	1
-2	A2E24, 22, 21, 20, 18, 16, 15, 13,	70934284001		SWITCH PUSH-ROCKER DPDT: 60A ac; 0.5A dc.	16
-3	12, 11, 09, 08, 07, 05, 03, 02, 01	70934283001		SWITCH PUSH SPDT.	1
-4	A2F2	70934287001		PUSHBUTTON LIGHT INDICATOR ASSEMBLY.	1
-5	A2F4	7093428801		SWITCH, LEVER LOCKING: 3 position, 3A, 200W	1
-6	A2F06, 08, 17, 18, 19, 20	70934285001		SWITCH, PUSH, ROCKER - SPDT; 6A at 125 Vac, 3A at 250 Vac; 1.0A dc.	6
-7	A2F07	70934285002		SWITCH, PUSH, ROCKER - SPDT: 6A at 125 Vac; 3A at 250 Vac; 1.0A dc.	1
-8	A2F10, 11, 12, 13, 14	70934286001		PUSHBUTTON ASSEMBLY.	1

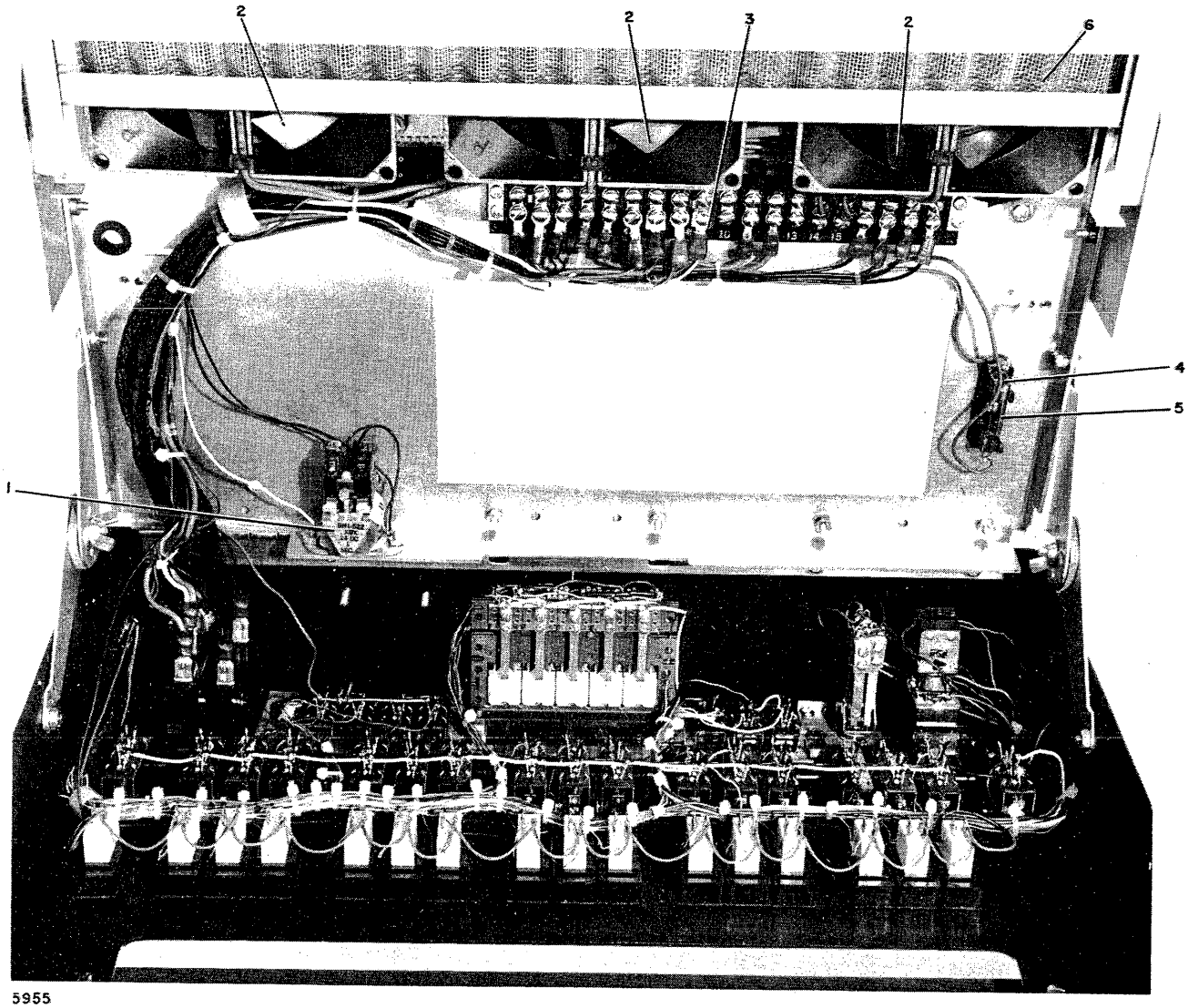


Figure 4-7. Chassis Assembly, Type 316-01

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-7-	A4	70023235701	B	CHASSIS ASSEMBLY, TYPE 316-01 (Refer to Figures 4-1-2 and 4-2-2 for NHA).	Ref
-1	A4E03	70963015007	C	RELAY ARMATURE - DPDT: 1 sec delay; contacts rated 5A, 125/250Vac; coils 24 Vdc, 2W continuous duty.	1
-2	A4B03, 06, 08	70964007001	C	FAN AXIAL: 4.13 in. square by 1.970 in. thick.	3
-3	A4C07	70937502019	C	TERMINAL BOARD: barrier type; 19 terminals; 20A rated, black molded bakelite.	1
-4	A4D09	7096002005	C	FUSE, CARTRIDGE: 0.5A; 250V; 1/4 in. diameter by 1-1/4 in. long instantaneous - Littelfuse 312.500.	1
-5	A4D09	70935008001	C	FUSEHOLDER: indicating types accom. 1/4 in. by 1-1/4 diameter fuse, rated 30A at 90 to 250V.	1
-6		70911003701	C	FILTER, AIR CONDITIONING.	1

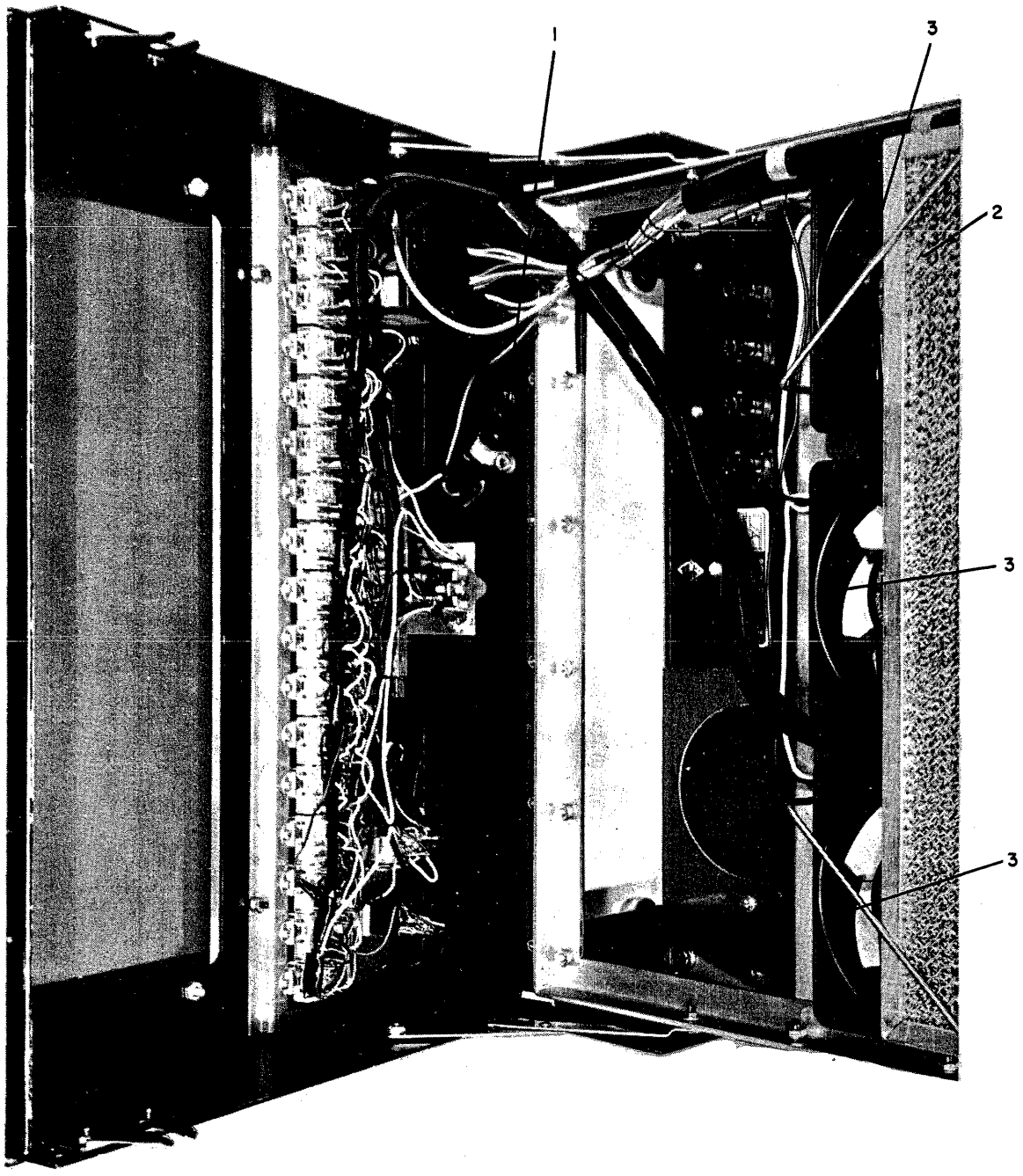


Figure 4-8. Chassis Assembly, Types 316-0100 and 316-0110

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-8-	A4	70030054701	B	CHASSIS ASSEMBLY, TYPES 316-0100 and 316-0110 (Refer to Figures 4-2-2 and 4-4-2 for NHA).	Ref.
-1		70960002005	C	FUSE, CARTRIDGE: 0.5A; 250V; 1/4 in. diameter by 1-1/4 in. long instantaneous Littelfuse 312.500.	1
		70935011002	C	FUSEHOLDER, IN-LINE: indicating types accom. 1/4 in. by 1-1/4 in. diameter fuse, rated 30A at 90 to 250V.	1
-2		70911003009	C	FILTER, AIR CONDITIONING.	1
-3	A4B03, 06, 08	70964008006	C	FAN, AXIAL: 4.13 in square by 1.970 in. thick.	

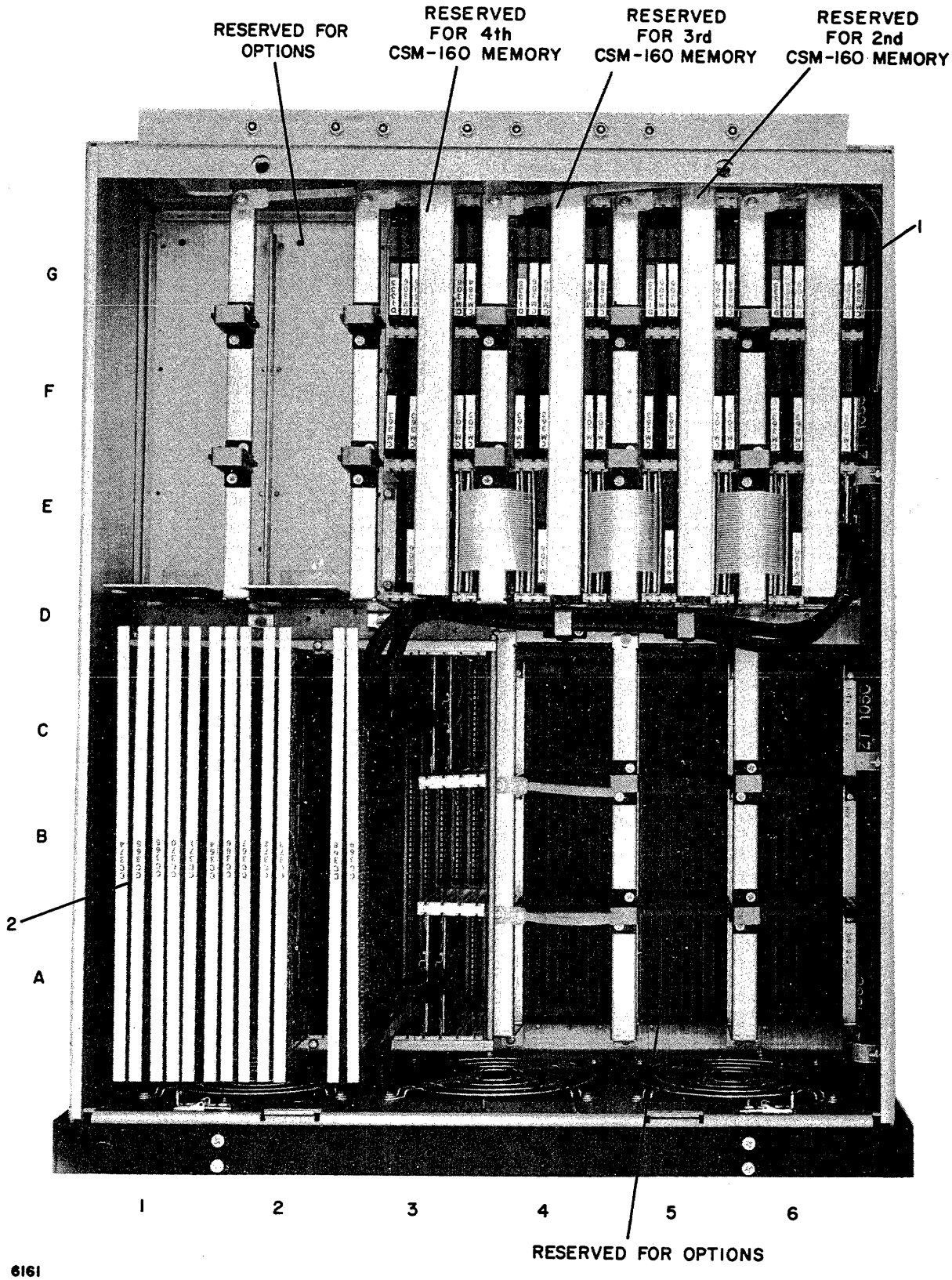


Figure 4-9. Mainframe Logic and Option Drawer Assembly, Type 316-01

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-9-	A1	70023232701	B	LOGIC AND OPTION DRAWER ASSEMBLY, TYPE 316-01 (Refer to Figures 4-1-3 and 4-4-4 for NHA).	Ref
-1		70023577704	C	CORE MEMORY UNIT (see Figures 4-11 and 4-12 for breakdown).	1
-2		No number	C	LOGIC PAC LAYOUT (see Figure 4-13 for breakdown).	1

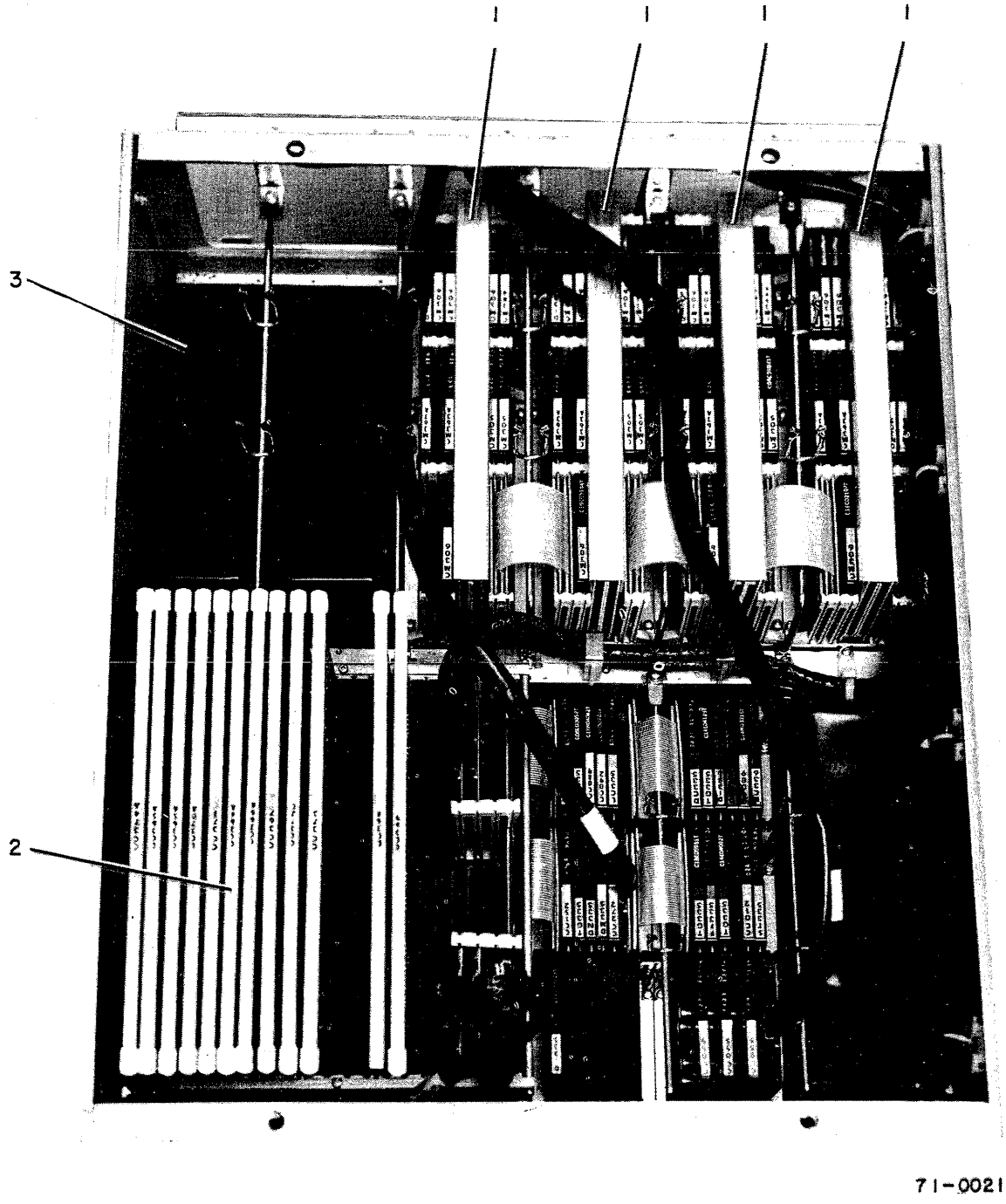


Figure 4-10. Mainframe Logic and Option Drawer Assembly, Types 316-0100 and 316-0110

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-10-	A1	70030064701	B	LOGIC AND OPTION DRAWER ASSEMBLY, TYPES 316-0100 and 316-0110 (Refer to Figures 4-2-3 and 4-4-4 for NHA).	Ref
-1		70023577704	C	CORE MEMORY UNIT (see Figures 4-11 and 4-12 for breakdown).	1
-2		No number	C	LOGIC PAC LAYOUT (see Figure 4-13 for breakdown).	1
-3		70030069001		PLATE FILLER.	Ref

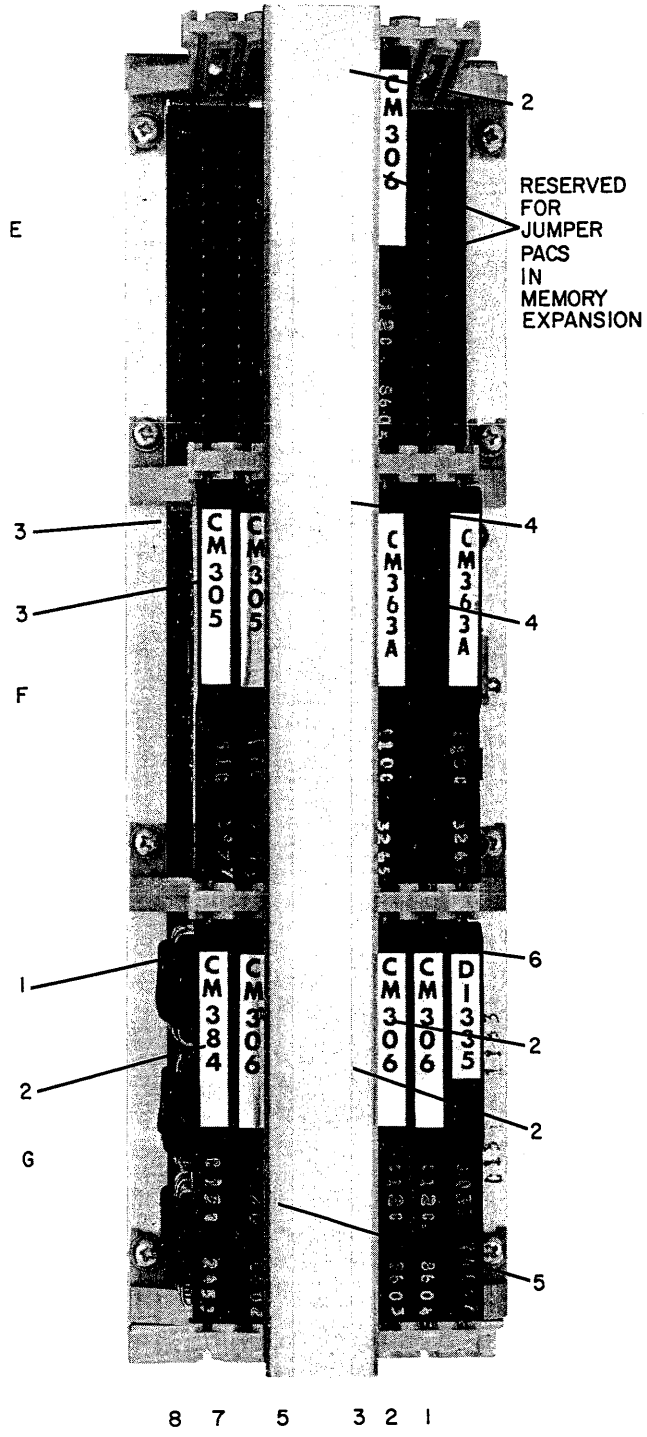


Figure 4-11. CSM-160 Core Memory Unit, Types 316-01, 316-0100, and 316-0110

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-11-	AIE-G	70023577	C	CSM-160 CORE MEMORY UNIT (Refer to Figure 4-10-1 for NHA).	Ref
-1	A1G608	CM-384	D	RESISTOR PAC (see Chapter II, Section 5 for breakdown).	1
-2	A1G607, A1E603, A1G602, A1G603	CM-306	D	SELECTOR PAC (see Chapter II, Section 5 for breakdown).	4
-3	A1F607, 08	CM-305	D	INHIBIT PAC (see Chapter II, Section 5 for breakdown)	2
-4	A1F601, 03	CM-363A	D	SENSE AMPLIFIER PAC (see Chapter II, Section 5 for breakdown).	2
-5	A1G04 A1G05	70	D	CORE STACK: 4096 words, 16 bits per word.	1
-6	A1G601	DI-375	D	NAND PAC (See Chapter II, Section 5, for breakdown).	1

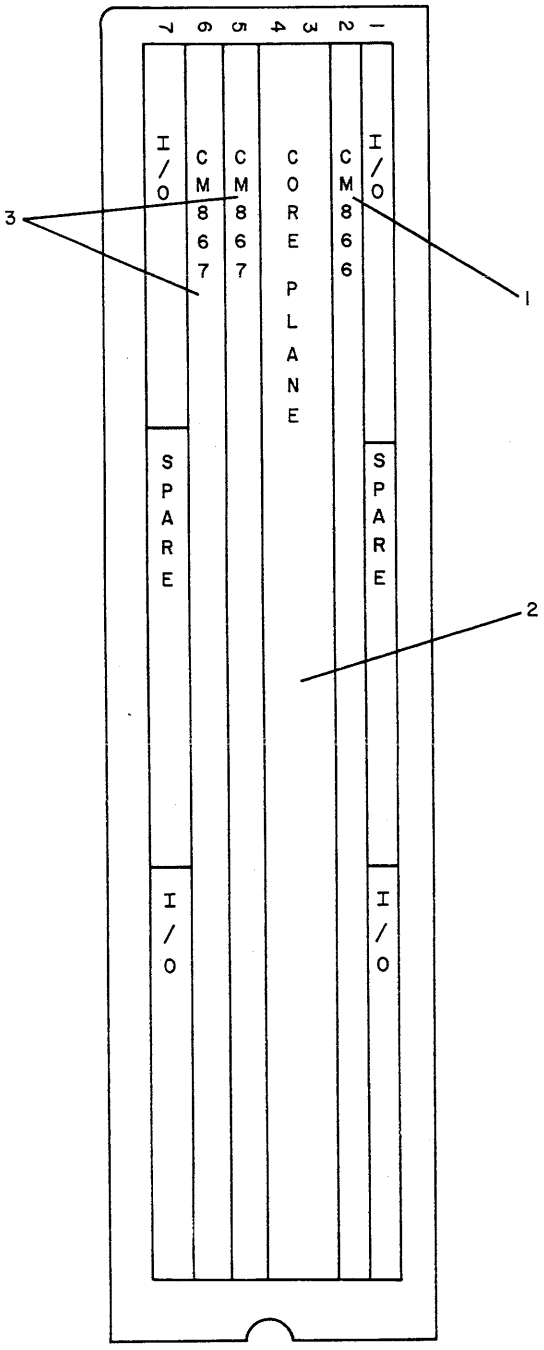


Figure 4-12. CSM-150 Core Memory Unit, Types 316-01, 316-0100, and 316-0110

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-12-	AIE-G	70032935	C	CSM-150 CORE MEMORY UNIT (Refer to Figure 4-10-1 for NHA).	Ref
-1	A1E602	CM-866	D	ADDRESS BOARD (see Chapter III, Section 10 for breakdown).	1
-2	A1E603 A1E604	70	D	CORE STACK: 8192 words, 17 bits per word.	1
-3	A1E605 A1E606	CM-867	D	DATA BOARD (See Chapter III, Section 10 for breakdown).	2

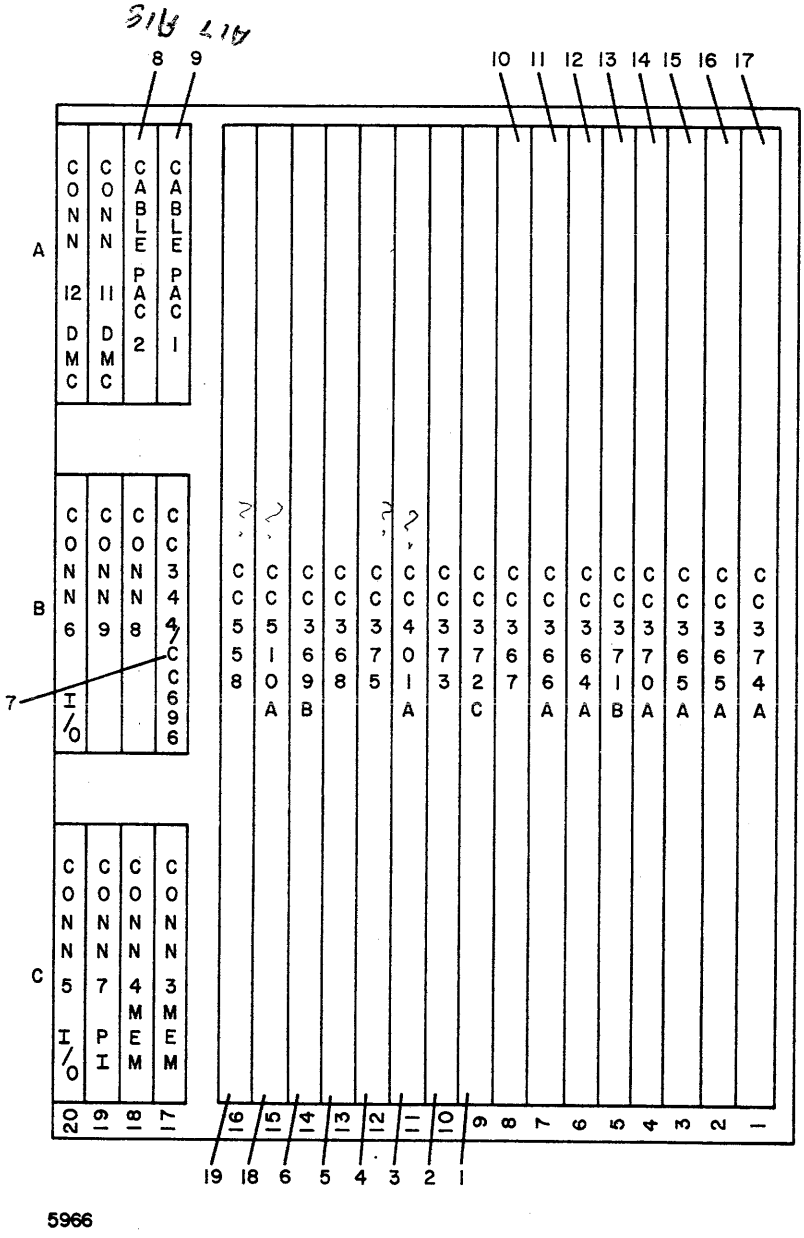


Figure 4-13. Logic Module Layout

Fig. & Index No.	Designation	Part No.	Indenture	Description	Qty per Ass'y
4-13-	A1BA	No Number	C	LOGIC PAC LAYOUT - PAC SIDE VIEW (Refer to Figure 4-9-2 and 4-10-2 for NHA).	Ref
-1	A1AA09	CC-372C	D	REGULATOR COUNTER MODULE (See Chapter I, Section 2 for breakdown).	1
-2	A1AA10	CC-373	D	MEMORY MODULE (See Chapter I, Section 2 for breakdown).	1
-3	A1AA11	CC-401	D	HIGH SPEED A-U No. 2 MODULE (See Chapter I, Section 2 for breakdown).	1
-4	A1AA12	CC-375	D	HIGH SPEED A-U No. 1 MODULE (See Chapter I, Section 2 for breakdown).	1
-5	A1AA13	CC-368	D	SHIFT REGISTOR MODULE (See Chapter I, Section 2 for breakdown).	1
-6	A1AA14	CC-369B	D	LAMP DRIVER MODULE (See Chapter I, Section 2 for breakdown).	1
-7	A1BA17	CC-344/ CC-696	D	REAL TIME CLOCK PAC (See Real Time Clock Option Instruction Manual Doc. No. 70130072179A for breakdown).	1
-8	A1AA18	CC-080 CC-681*	D	CABLE PAC (See Chapter I, Section 2 for breakdown).	1
-9	A1AA17	CC-079 CC-672*	D	CABLE PAC (See Chapter I, Section 2 for breakdown).	1
-10	A1AA08	CC-367	D	ADDRESS BUS MODULE (See Chapter I, Section 2 for breakdown).	1
-11	A1AA07	CC-366A	D	COLUMNS 9-12 MODULE (See Chapter I, Section 2 for breakdown).	1
-12	A1AA06	CC-364A	D	COLUMNS 1-4 MODULE (See Chapter I, Section 2 for breakdown).	1
-13	A1AA05	CC-371B	D	CLOCK MODULE (See Chapter I, Section 2 for breakdown).	1
-14	A1AA04	CC-370A	D	M REGISTOR MODULE (See Chapter I, Section 2 for breakdown).	1
-15, -16	A1AA02, 03	CC-365A	D	COLUMNS A-D MODULE (See Chapter I, Section 2 for breakdown).	2
-17	A1AA01	CC-374A	D	ASR INTERFACE MODULE (See Chapter I, Section 2 for breakdown)	1
-18	A1AA15	CC-510A	D		1
-19	A1AA16	CC-558	D		1

*Used in Type 316-0100 only

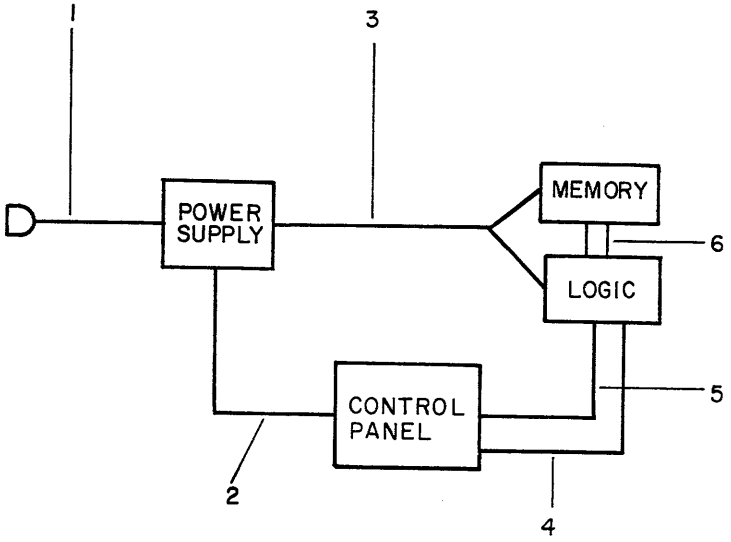


Figure 4-14. Cable Block Diagram

Fig. & Index No.	Type	Part No.	Indenture	Description	Qty per Ass'y
4-14-			A	CABLING BLOCK DIAGRAM.	Ref
-1	316-01	940252003	B	CABLE ASSEMBLY, POWER: Electrical, 12 ft overall length.	1
	316-0100	940252002	B	CABLE ASSEMBLY, POWER: Electrical, 9 ft overall length.	1
-2	316-01	70023838701	B	CABLE ASSEMBLY, POWER: Electrical Power Supply to Control Panel, 9 ft overall length (see Figure 4-15 for breakdown).	1
	316-0100	70030072703	B	CABLE ASSEMBLY, POWER: Electrical Power Supply to Control Panel; 9 ft overall length (see Figure 4-16 for breakdown).	1
-3	Both types	70023837705	B	CABLE ASSEMBLY, POWER: Electrical Power Supply to Logic Drawer, 10 ft. overall length (see Figure 4-17 for breakdown).	1
-4	316-01	7024016701	B	CABLE ASSEMBLY, SPECIAL PURPOSE: Control Panel Cable No. 1 (see Figure 4-18 for breakdown).	1
	316-0100	70029942701	B	CABLE ASSEMBLY, SPECIAL PURPOSE: Control Panel Cable No. 1 (see Figure 4-19 for breakdown).	1
-5	316-01	7024010701	B	CABLE ASSEMBLY, SPECIAL PURPOSE: Control Panel Cable No. 2 (see Figure 4-20 for breakdown).	1
	316-0100	70029943701	B	CABLE ASSEMBLY, SPECIAL PURPOSE: Control Panel Cable No. 2 (see Figure 4-21 for breakdown).	1
-6	Both types	70032670703	B	CABLE ASSEMBLY, SPECIAL PURPOSE: μ-PAC to μ-PAC, 2 ft overall length (see Figure 4-22 for breakdown).	2

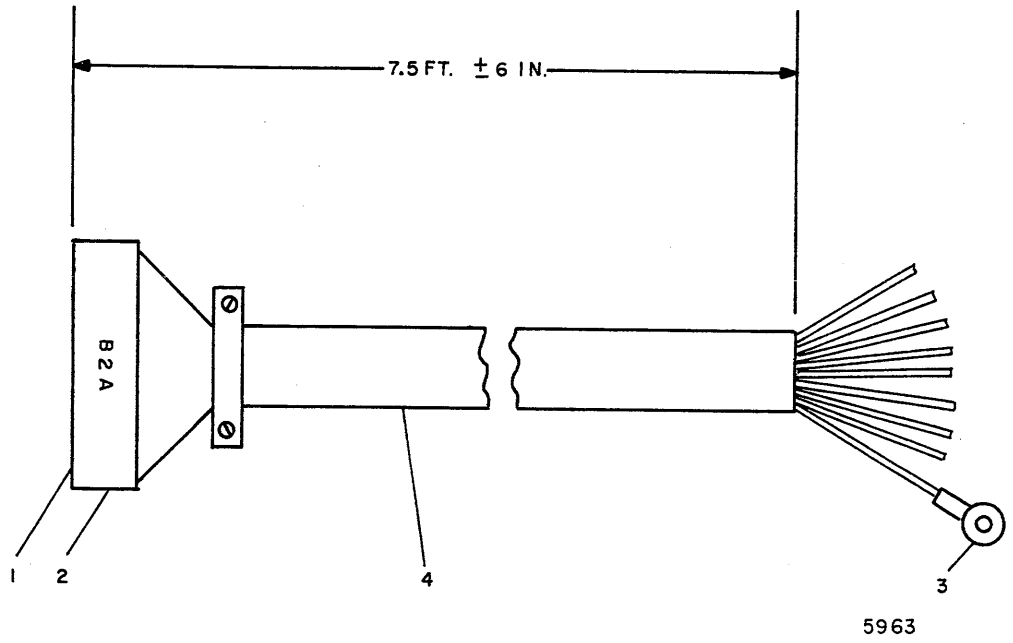


Figure 4-15. Cable Assembly, Power, Electrical, Type 316-01

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-15-		7023838701	B	CABLE ASSEMBLY, POWER: Electrical (Refer to Figure 4-14-2 for NHA).	Ref
-1	B2A	70941371001	C	CONNECTOR, PLUG, ELECTRICAL.	1
-2		70941571001	C	PLUG TIP, MALE.	15
-3	AXC	70937058003	C	TERMINAL LUG.	15
-4		70981002024	C	SLEEVING, ELECTRICAL.	8 ft

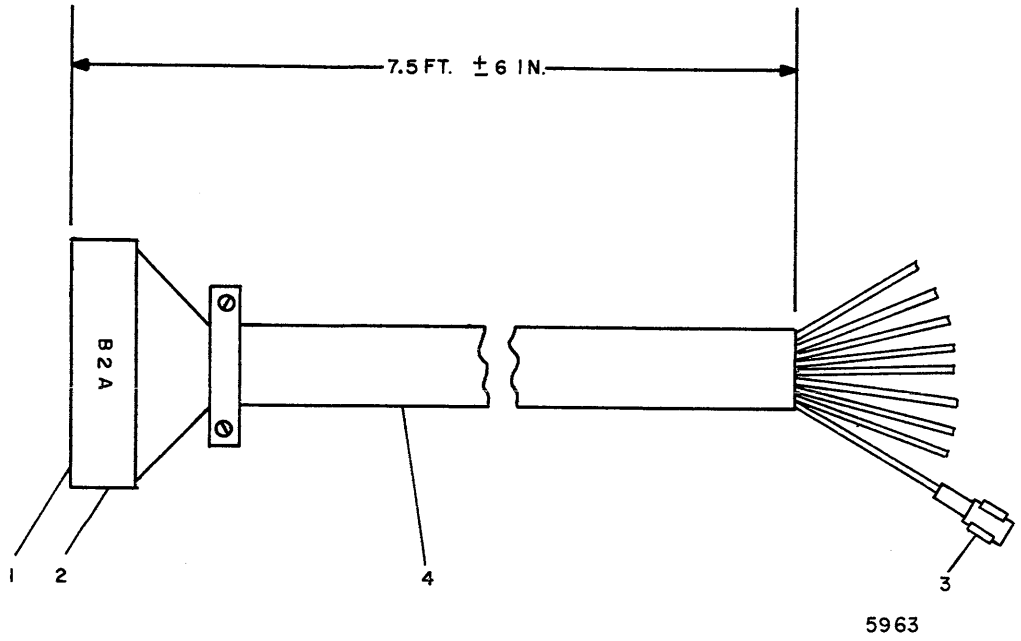


Figure 4-16. Cable Assembly, Power, Electrical, Types 316-0100 and 316-0110

Fig. & Index No.	Designation	Part No.	Indenture	Description	Qty per Ass'y
4-16-		70030072703	B	CABLE ASSEMBLY, POWER: Electrical (Refer to Figure 4-14-2 for NHA).	Ref
-1	B2A	70941341003	C	CONNECTOR, PLUG, ELECTRICAL.	1
-2		70941571001	C	PLUG TIP, MALE.	15
-3	AXC	70937200001	C	TERMINAL.	6
-4		70981002021	C	SLEEVING, ELECTRICAL.	9 Ft

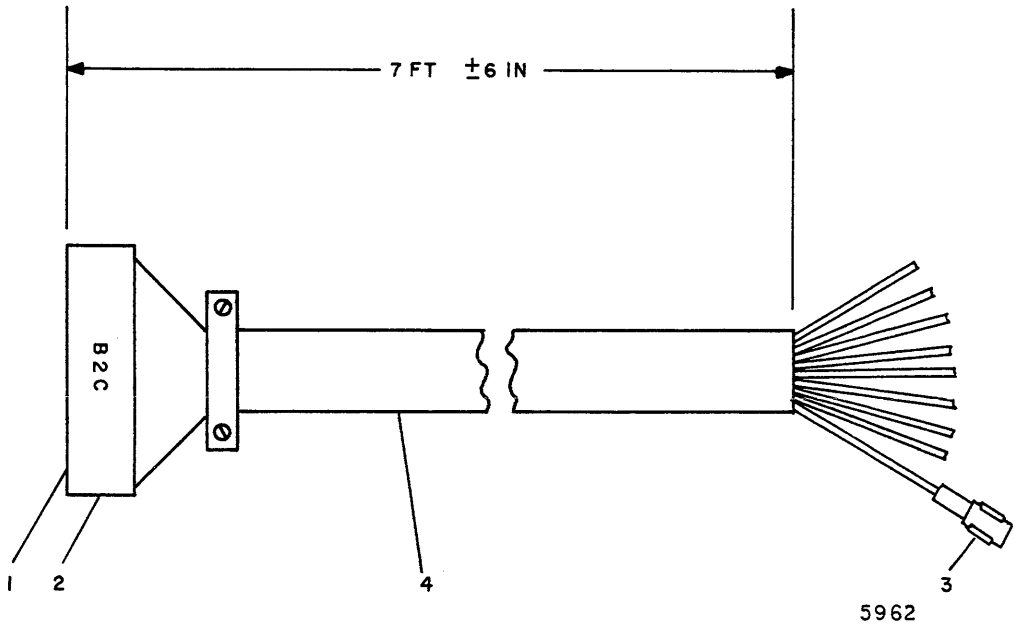


Figure 4-17. Cable Assembly, Power, Electrical, Types 316-01, 316-0100 and 316-0110

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-17-		7023837705	B	CABLE ASSEMBLY, POWER: Electrical (Refer to Figure 4-14-3 for NHA).	Ref
-1	B2C	70941341001	C	CONNECTOR, PLUG, ELECTRICAL.	1
-2		70941571001	C	PLUG TIP, MALE.	13
-3	A1D	70937200001	C	TERMINAL, QUICK DISCONNECT.	11
-4		70981002023	C	SLEEVING, ELECTRICAL.	8 Ft

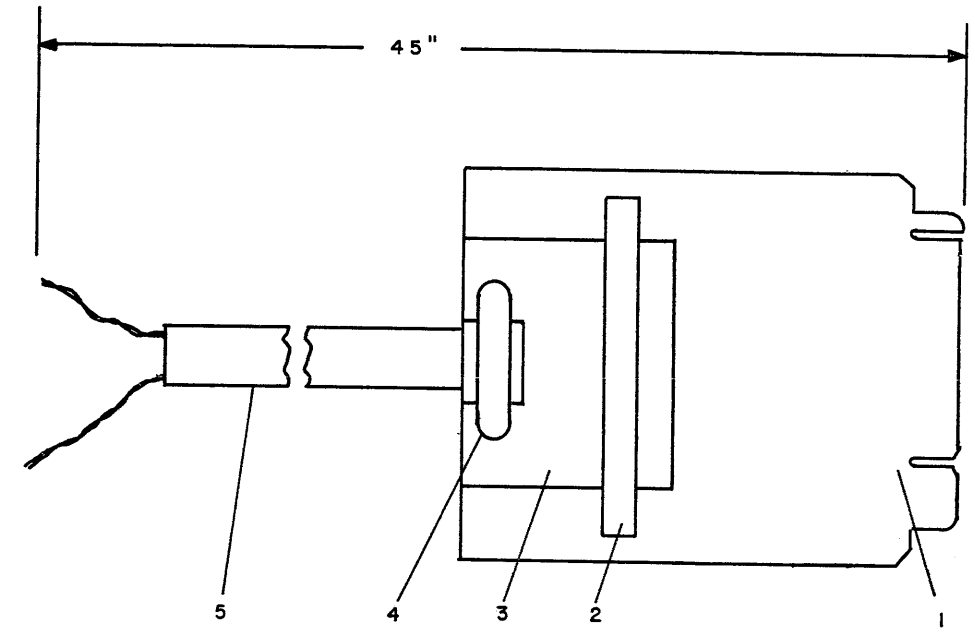


Figure 4-18. Cable Assembly, Special Purpose, Control Panel Cable No. 1, Type 316-01

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-18-		70024016701	B	CABLE ASSEMBLY, SPECIAL PURPOSE, CONTROL PANEL CABLE NO. 1, TYPE 316-01 (Refer to Figure 4-14-4 for NHA).	Ref
-1	A1AA17	CC-079	C.	CABLE PAC (See Figure 4-13-9 for PAC location and Chapter I, Section 2 for breakdown).	Ref
-2		70013624001	C	BRACKET, CLAMPING.	1
-3		70013626001	C	PLATE.	1
-4		70013623001	C	CLAMP.	1
-5		70940359001	C	CABLE, SPECIAL, ELECTRICAL.	4 Ft

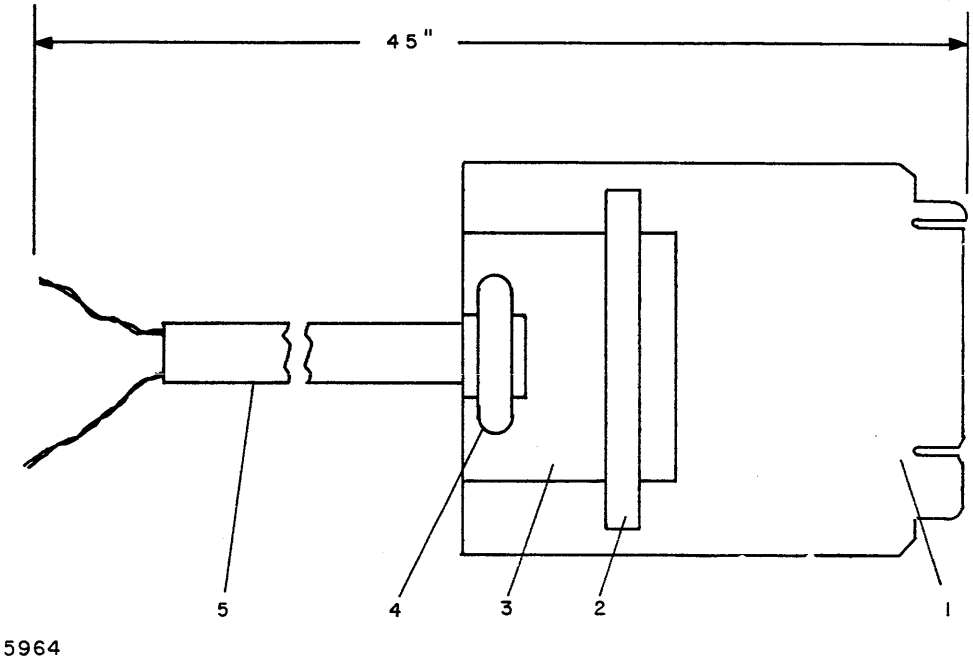


Figure 4-19. Cable Assembly, Special Purpose, Control Panel Cable No. 1, Types 316-0100 and 316-0110

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-19-		70029942701	B	CABLE ASSEMBLY SPECIAL PURPOSE, CONTROL PANEL CABLE NO. 1, TYPES 316-0100 and 316-0110 (Refer to Figure 4-14-4 for NHA).	Ref
-1	A1AA17	CC-672	C	CABLE PAC (See Figure 4-13-9 for PAC location and Chapter 1, Section 2 for breakdown).	Ref
-2		70013624001	C	BRACKET, CLAMPING.	1
-3		70029335001	C	PLATE.	1
-4		70029261001	C	CLAMP.	1
-5		70940161001	C	CABLE, SPECIAL, ELECTRICAL.	4 Ft

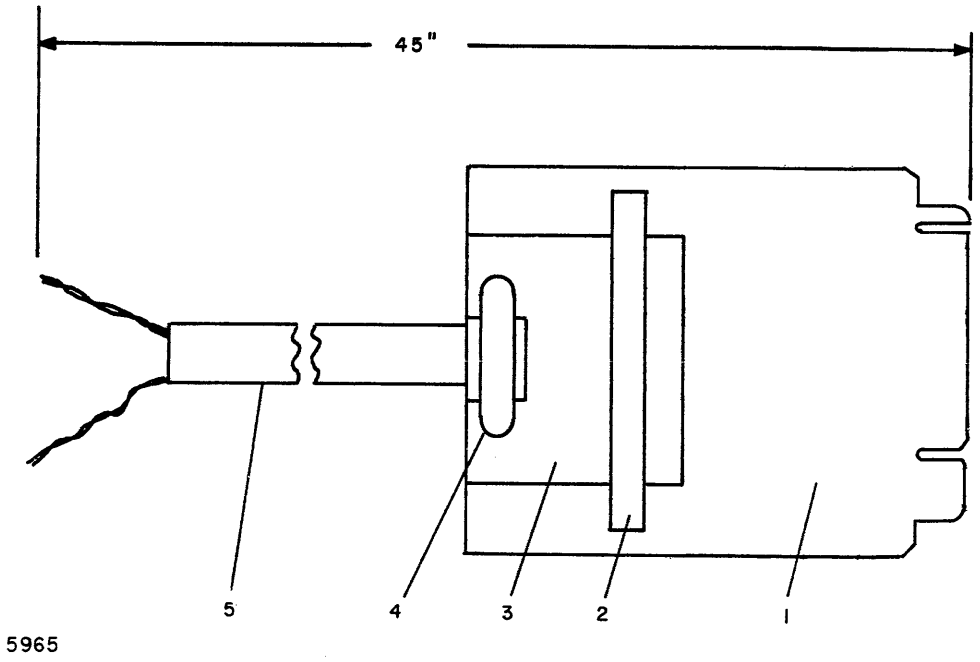


Figure 4-20. Cable Assembly, Special Purpose, Control Panel Cable No. 2, Type 316-01

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-20-		70024010201	B	CABLE ASSEMBLY, SPECIAL PURPOSE, CONTROL PANEL CABLE NO. 2, TYPE 316-01 (Refer to Figure 4-14-5 for NHA).	Ref
-1	A1AA18	CC-080	C	CABLE PAC (See Figure 4-13-8 for PAC location and Chapter I, Section 2 for breakdown).	Ref
-2		70013624001	C	BRACKET, CLAMPING.	1
-3		70013626001	C	PLATE.	1
-4		70013623001	C	CLAMP.	1
-5		70940359001	C	CABLE, SPECIAL, ELECTRICAL.	4 Ft

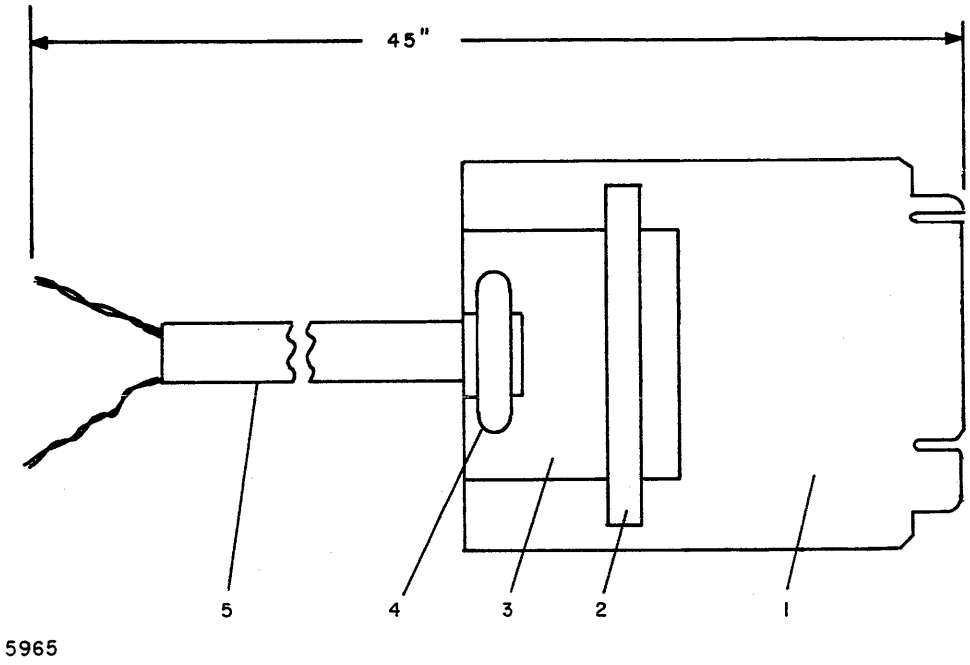


Figure 4-21 Cable Assembly, Special Purpose, Control Panel Cable No. 2, Types 316-0100 and 316-0110

Fig. & Index No.	Desig-nation	Part No.	Inden-ture	Description	Qty per Ass'y
4-21-		70029943701	B	CABLE ASSEMBLY, SPECIAL PURPOSE, CONTROL PANEL CABLE NO. 2, TYPES 316-0100 and 316-0110 (Refer to Figure 4-14-5 for NHA).	Ref
-1	A1AA18	CC-681	C	CABLE PAC (See Figure 4-13-8 for PAC location and Chapter I, Section 2 for breakdown).	Ref
-2		70013624001	C	BRACKET, CLAMPING.	1
-3		70029335001	C	PLATE.	1
-4		70029261001	C	CLAMP.	1
-5		70940159001	C	CABLE, SPECIAL, ELECTRICAL.	4 Ft.

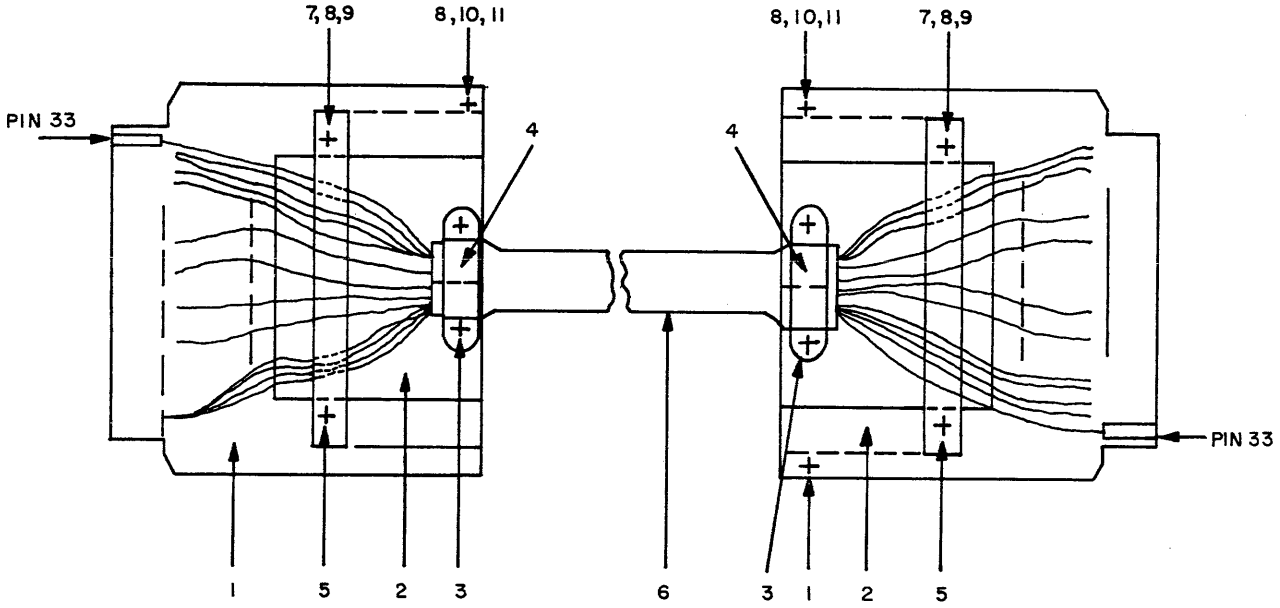


Figure 4-22. Cable Assembly, Special Purpose, μ-PAC to μ-PAC, for Types 316-01, 316-0100, and 316-0110 (Drawing No. A70032670 Rev C)

Fig. & Index No.	Designation	Part No.	Indenture	Description	Qty per Ass'y
4-22-		70032670703	B	CABLE ASSEMBLY, μ-PAC to μ-PAC (Refer to Figure 4-14-6 for NHA).	Ref
-1		70013767701	B	PC CBL PAC.	2
-2		70013626001	B	Plate.	2
-3		70904109001	C	Screw, No. 2-56 x 1/8 in.	4
-4		70032671001	C	Clamp.	2
-5		70013624001	C	Bar, Clamping.	2
-6		70940377001	C	Cable, 32 Twisted Pair.	A/R
-7		70902050001	C	Washer, Flat, No. 2.	4
-8		70902006039	C	Washer, Lock, Split, No. 2.	12
-9		70982152003	C	Cable Marker.	2
-10		70904109002	C	Screw, No. 2-56 x 3/16 in.	8
-11		70902050002		Washer, Flat, No. 2.	4

ADDENDUM
TYPE 316/716 POWER DISTRIBUTION UNIT

SECTION 1
INTRODUCTION

GENERAL DESCRIPTION

The Type 316/716 Power Distribution Box is designed to provide 120 Vac one-phase 60 Hz power to Type 316/716 drawers, μ-PAC option drawers and various peripheral devices via standard parallel blade duplex outlets.

The unit takes two phases of a three-phase system and splits it into two single-phase branch circuits, on which are contained five individual fused outlets.

SPECIFICATIONS

Electrical Specifications

Input Voltage. -- The input voltage to the power distribution box is a 208 Vac three-phase 60 Hz 5 wire service.

Input Current. -- Loading on the input lines will be from phase to neutral on two-phase only. The maximum load current per phase will be 24A, and there is no provision or procedure for balancing the load on the phase. The unused phase is terminated at the input connector and for possible future expansion.

Output Voltages and Currents. -- The voltage provided by each output connector is normally 120 Vac one-phase 60 Hz, and the maximum current that can be obtained from each duplex connector is 15A.

Power On/Off. -- The power distribution box is turned on and off by means of a 120 Vac control line from a Type 316/716 power supply or similar source which controls a two-pole contact within the box.

Mechanical Specifications

The dimensions of the power distribution are:

Length: 16.475 inches

Width: 19 inches

Height: 5.22 inches

The power distribution box consists of the following:

Sheet metal chassis

Input converter

Contacts

Five output converters

Five output Edison base fuses

Input circuit breaker

Input and output RFI filters.

The input and output connectors are mounted on the rear of the PD box: the circuit breaker and fuses are on the front. The contactor is attached to the inside of the front panel, and the RFI filters are located near the right side at the bottom of the box.

SECTION 2
OPERATING PROCEDURES

CONTROLS AND INDICATORS

There are no controls or indicators on the power distribution box.

OPERATING GUIDES

For personnel safety, do not replace fuses with the input circuit breaker in the ON position.

SECTION 3
FUNCTIONAL THEORY OF OPERATION

BLOCK DIAGRAM ANALYSIS

The block diagram of the power distribution box is shown in Figure A-1.

The ac input power enters the power distribution box through J8 and passes through an RFI filter to the circuit breaker. From there it goes to the contactor and J7 via a fuse. When the contactor is energizing by J6, power is provided to J1 through J5 via 15A fuses. J1 has an additional RFI filter for load which could generate noise onto the ac line.

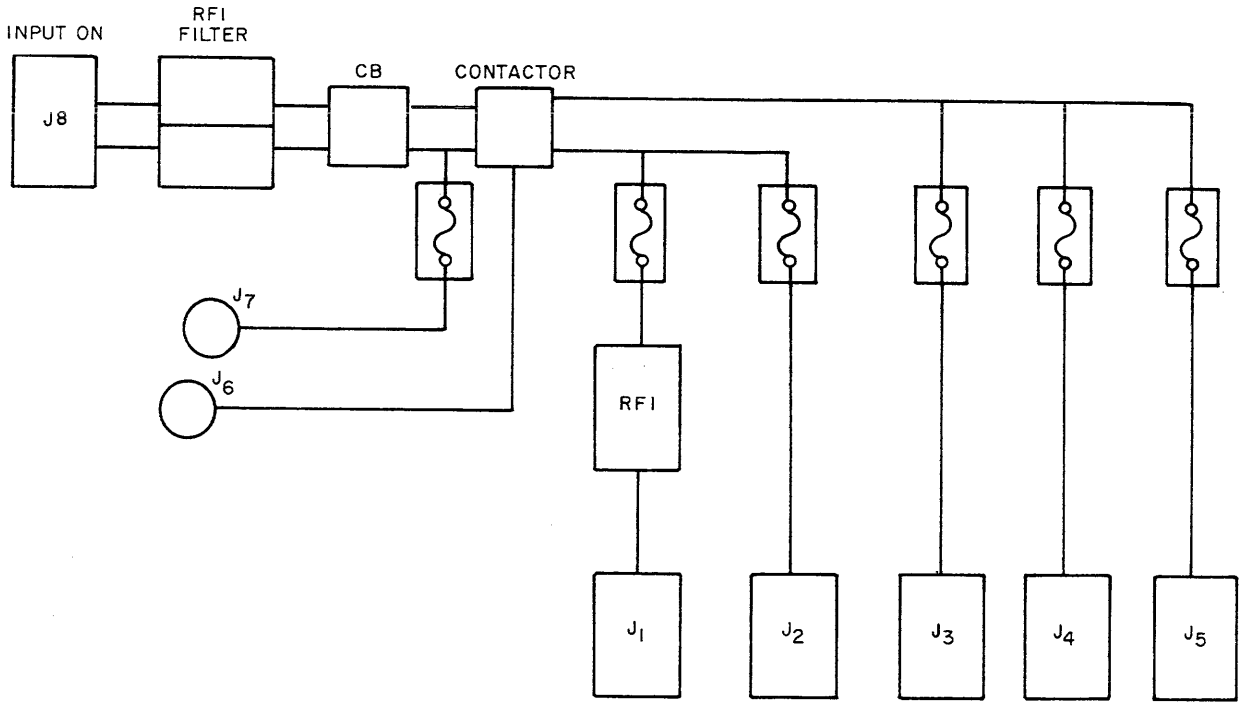


Figure A-1. Power Distribution Unit Block Diagram

SECTION 4
DETAILED THEORY OF OPERATION

DETAILED LOGIC DESCRIPTION

Refer to Figure A-3 for schematics. The power distribution box is designed to take two phases of a three-phase input power line and divide into two single-phase branch circuits for the operation of any Type 316/716 equipment which requires 120 Vac via a standard parallel blade plug.

J8 brings into the box two phases, neutral and earth ground. Earth ground (pin GR) is connected to the box by an integral stud which is also connected to the ground terminals of J1 through J7. The neutral line, Pin W, is wired directly to "cold" side of each connector (silver colored terminal). The two phases (pins X and Y) are each wired to a pi section RFI filter and then to a two-pole community circuit breaker. Thus, if a fault occurs in one phase, the other will also be disconnected. The breaker will trip for currents in excess of 24A. The output of the circuit breaker is wired to a two-pole contactor and one leg is also wired to J7 through a 15A fuse. The output of the contactor is wired to the "hot" side of the duplex outlet (brass color). When used in a Type 316/716 system, a Type 316/716 power supply is plugged into J7 and a cable from the duplex outlet on the Type 316/716 power supply is plugged into J6. With the circuit breaker in the ON position, power is applied to J7 and the switch on the Type 316/716 control panel which is plugged into J7 via the power supply. When the switch is turned on, the duplex outlet on the supply energizes the contactor through J6 thus applying power to J7 through J5 on the PD box. Conversely, when the switch on the control panel is turned off, power is also removed from the outlet on the PD box.

INTERFACE

Primary Power Interface

The ac input connector on the power distribution box, J8, mates with a Hubbell Model No. 25414 or equivalent.

Output Power Interface

J1 through J5 will mate with any parallel blade plug (i.e., Hubbell Cap. 5200 series or 5900 series).

Control Interface

J7 mates with any parallel blade plug (i.e., Hubbell Caps, 5200 series or 5900 series). J6 mates with a Hubbell Model No. 4730-K twist lock connector or equivalent.

SECTION 5
INSTALLATION

PRELIMINARY INFORMATION

Service personnel should be familiar with the complete installation procedure and safety precautions before attempting to install the Type 316/716 power distribution box.

Tools and Test Equipment

A medium size screwdriver is all that is required to install the Power Distribution Unit.

Space and Environmental Requirements

The space and environmental requirements are presented in the Mechanical Specification paragraph.

INTERFACE CONSIDERATIONS

Interface considerations are presented in the Electrical Specification.

INSTALLATION PROCEDURE

Mechanical Procedure

Refer to Figure A-2.

Electrical Interconnections

Refer to the Site Planning Manual (order no. AD71) for the input ac connection. For additional cabling information, refer to Table A-1 (wire list).

CHECKOUT PROCEDURE

Initial Checkout

Before plugging in power, check all fuses. Check that circuit breaker is in the OFF position, and check that all plugs to the Type 316/716 power supply are firmly seated in their pockets.

Cycle-up Checkout

Plug in ac connector and operate power switch on control panel. Check for 120Vac with ac voltmeter at each duplex output.

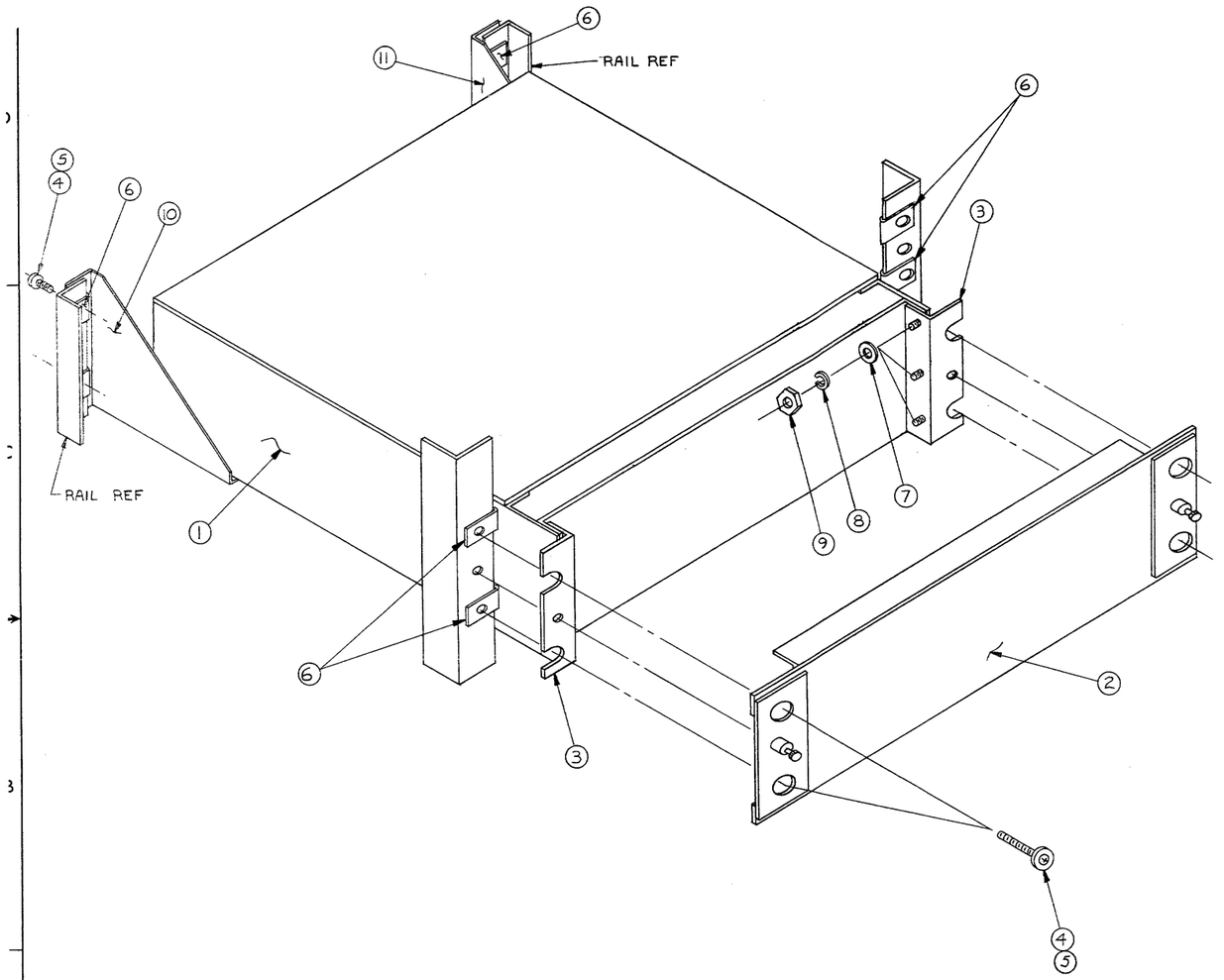
On-Line Checkout

Connect cables to duplex outlet and apply power via control panel. Check each device plugged into box for presence of ac power.

SECTION 6
MAINTENANCE

EQUIPMENT CONFIGURATION

Figure A-2 presents the installation and accessories drawing.



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	PER S.R. 7725-0058 ISSUED PER DIN 74384	11	11

3. LOCATION OF UNIT TO BE IN ACCORDANCE WITH 70110011598 SECTION III.

2. BEFORE TIGHTENING OF ITEM 4 ASSEMBLE ITEM 2 TO ITEM 3 TO ASSURE ALIGNMENT OF ITEM 2 TO ITEM 4.

1. ASSEMBLE ITEMS 1 & 3 USING ITEMS 7, 8 & 9.

701

UNSPECIFIED TOLERANCES	REQD PER UNIT	REQD PER UNIT	ITEM NO.	DRAWING NUMBER	DESCRIPTION	GOVT. NO
	—	—		P70033043	PARTS LIST	

SECTION 7
TROUBLESHOOTING

TROUBLESHOOTING PROCEDURES

The box should be given a good visible inspection for damage to internal parts and input and output connectors.

Recommended Test Equipment

Ac voltmeter, ac ammeter.

Check Procedure

If there is no output at any of the connectors, check the following:

a. Voltage present at input connector.
b. Blown 15A fuse of Type 316/716 power supply.
c. Control panel to Type 316/716 power supply cable not connected.
d. Loose cables at J6 and J3.
e. Defective contactor.
f. Defective circuit breaker.

If there is no voltage at an individual output connector, check 15A fuses on front of PD box.

If individual fuse blows continuously, check for overload or shunt at output connector.

WIRE LIST

The wire list is presented in Table A-1.

Refer to Interface paragraph for interface connections.

Table A-1.
PDU Wire List

From	To	Wire Color and Gage
XXAJ8--J0X	XXA10---01	BLK #10
XXAJ8--J0Y	XXA11---01	
XXAJ8--J0W	XXAJ1--J04	
XXA11---02	XXB07-CB04	
XXA11---02	XXB07-CB03	
XXB07-CB01	XXB08---02	
XXB07-CB02	XXB08---01	#10
XXBF6--F01	XXB08---02	BLK #14
XXB08---08	XXAJ6--P01	BLK
XXB08---07	XXAJ6--P02	BLK
XXBF1--F02	XXA09---01	RED
XXAJ2--J04	XXAJ7--J01	BLK
XXBF2--F02	XXAJ2--J02	RED
XXBF3--F02	XXAJ3--J02	RED
XXA09---02	XXAJ1--J02	BLK
XXBF2--F01	XXB08---05	BLK
XXBF3--F01	XXB08---06	BLK
XXBF4--F02	XXAJ4--J02	RED
XXBF4--F01	XXB08---06	BLK
XXBF5--F01	XXB08---06	BLK
XXBF5--F02	XXAJ5--J02	RED
XXBF6--F02	XXAJ7--J02	BLK #14
XXAJ1--J03	XXAJ2--J03	#10
XXAJ8--J0W	XXAJ3--J03	#10
XXAJ3--J04	XXAJ4--J04	#10
XXAJ4--J03	XXAJ5--J03	#14
XXBF1--F01	XXB08---05	BLK #14
XXAJ8--JGR	XXA12-GR01	GRN #10
XXA12-GR01	XXAJ01-J05	#14
XXAJ01-J05	XXAJ02-J05	
XXAJ02-J05	XXAJ03-J05	
XXAJ03-J05	XXAJ04-J05	
XXAJ04-J05	XXAJ05-J05	
XXAJ05-J05	XXAJ07-J03	
XXAJ07-J03	XXAJ06-J03	GRN #14

SECTION 8
REFERENCE DATA

PD UNIT SCHEMATIC (Figure A-3.)

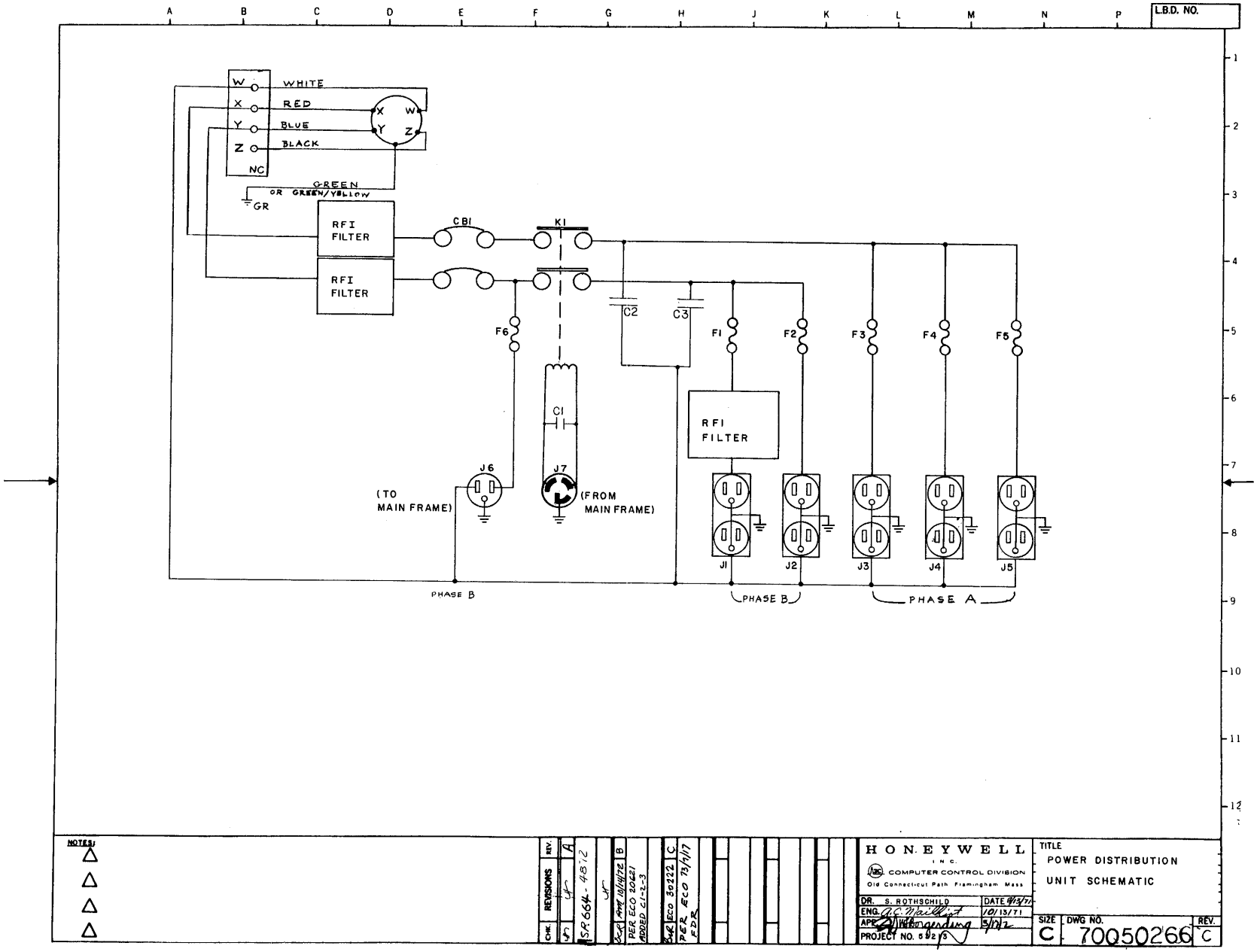


Figure A-3. Power Distribution Unit Schematic
(Ref. Drawing C70050266, Rev. C)

SECTION 9
ILLUSTRATED PARTS BREAKDOWN

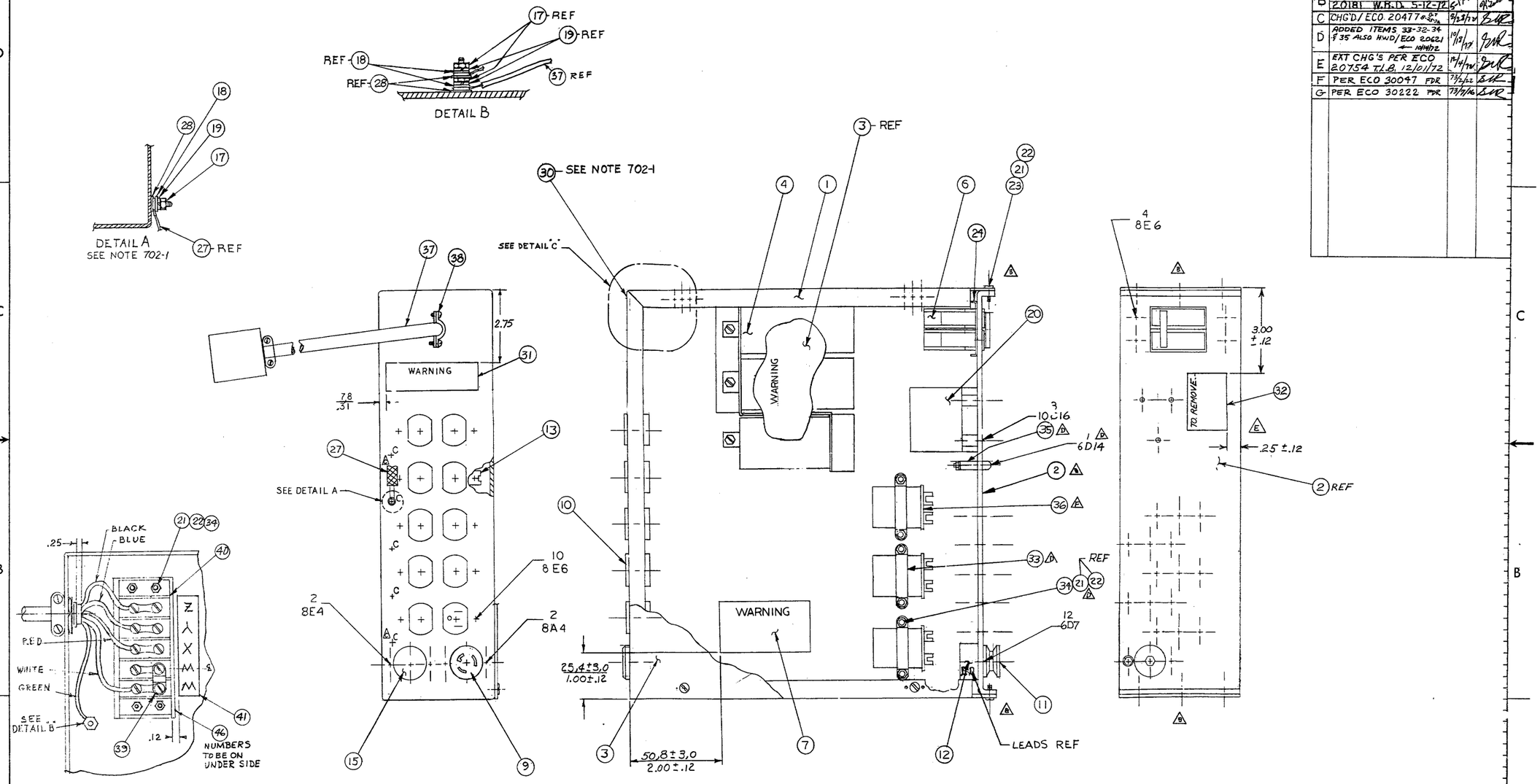
This section contains illustrated parts lists for the following power distribution unit assemblies.

	Table No.	Figure No.
Chassis Assembly	A-2	A-4
Coding Drawing	—	A-5

Table A-2.
Chassis Assembly Parts List
(See Figure A-4)

Item	Part Number	Description	Qty 702
01	7001954-702	CHASSIS, DET/ASSY	001
02	7001953-701	PANEL, FRONT DET/ASSY	001
03	70031806-701	COVER, PDU DET/ASSY	001
04	70942407-002	LINE FILTER	003
06	70960060-013	CIRCUIT BREAKER, CB 1	001
07	70982112-001	PLATE, IDENT	001
09	70941163-001	CONNECTOR, RECEPTACLE, ELECT, J7	001
10	70941323-001	CONNECTOR, RECEPTACLE, ELEC, J1-J5	005
11	04670063-029	FUSE-FUSTAT F1-F6	006
12	04670062-013	FUSE-HOLDER-FUSTAT	006
13	70901400-009	NUT, SHEET SPRING	010
15	70941334-001	CONNECTOR, RECEPTACLE, J6	001
17	70901005-002	NUT, #10-32	007
18	70902050-012	WASHER, FLAT, #10	007
19	70902006-043	WASHER, LOCK, #10	007
20	70963027-002	RELAY, SOLENOID, K1	001
21	70902006-042	WASHER, LK, #8-32	016
22	70902050-010	WASHER, FLAT, #8-32	016
23	70904113-046	SCREW, #8-32	006
24	70960060-102	CIRCUIT BREAKER, MTG BRKT	001
27	70032069-702	GROUND STRAP	001
28	70902003-032	WASHER, EXT, TOOTH #10	007
30	70032183-000	ONE-LINE DIAGRAM	001
31	70982128-003	PLATE, IDENT	001
32	70982131-001	PLATE, IDENT	001
33	70906164-001	CLAMP, CAP	003
34	70901003-006	HEX, NUT, 8-32	006
35	70908052-131	SPACER	001
36	04310020-015	CAP	003
37	70032761-702	CABLE, POWER	001
38	03510051-003	CLAMP, CABLE	001
39	70908035-004	CLIP, ELECT	001
40	70937506-005	BOARD, TERM	001
43	70031997-702	WIRE LIST	001
44	70033072-000	SCHEMATIC PDV	REF
45	70033073-000	CODING, DWG	REF
46	70982006-005	PLATE, DESIG	001

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	PER SR 664-4872		
B	EXT CHG'S / ECO 20181 W.R.D. 5-12-72	6-17-72	
C	CHG'D/ECO 20477	8/23/72	
D	ADDED ITEMS 33-32-34 & 35 ALSO HWD/ECO 20621 ← 14948-72	10/3/72	
E	EXT CHG'S PER ECO 20754 T.L.B. 12/01/72	12/4/72	
F	PER ECO 30097 FDR	7/12/73	
G	PER ECO 30222 FDR	7/17/73	



1. MOUNTING OF HARDWARE, ITEMS 17, 18, 19 & 28, 5 PLCS MKD C. ITEM 27 TO BE INSTALLED IN ONE C LOCATION AS SHOWN IN DETAIL A.

702

UNSPECIFIED TOLERANCES		
	METRIC	INCHES
1 PLACE	±0,5	
2 PLACE	±0,13	± .02
3 PLACE		±.005

THIRD ANGLE PROJECTION

LINEAR MEASURE: MM / IN.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
DECIMALS ± .005 IS PLACED
.03 IS PLACED
ANGLES ± 1/2°
FASTENER ASSEMBLY PER 122 801 027

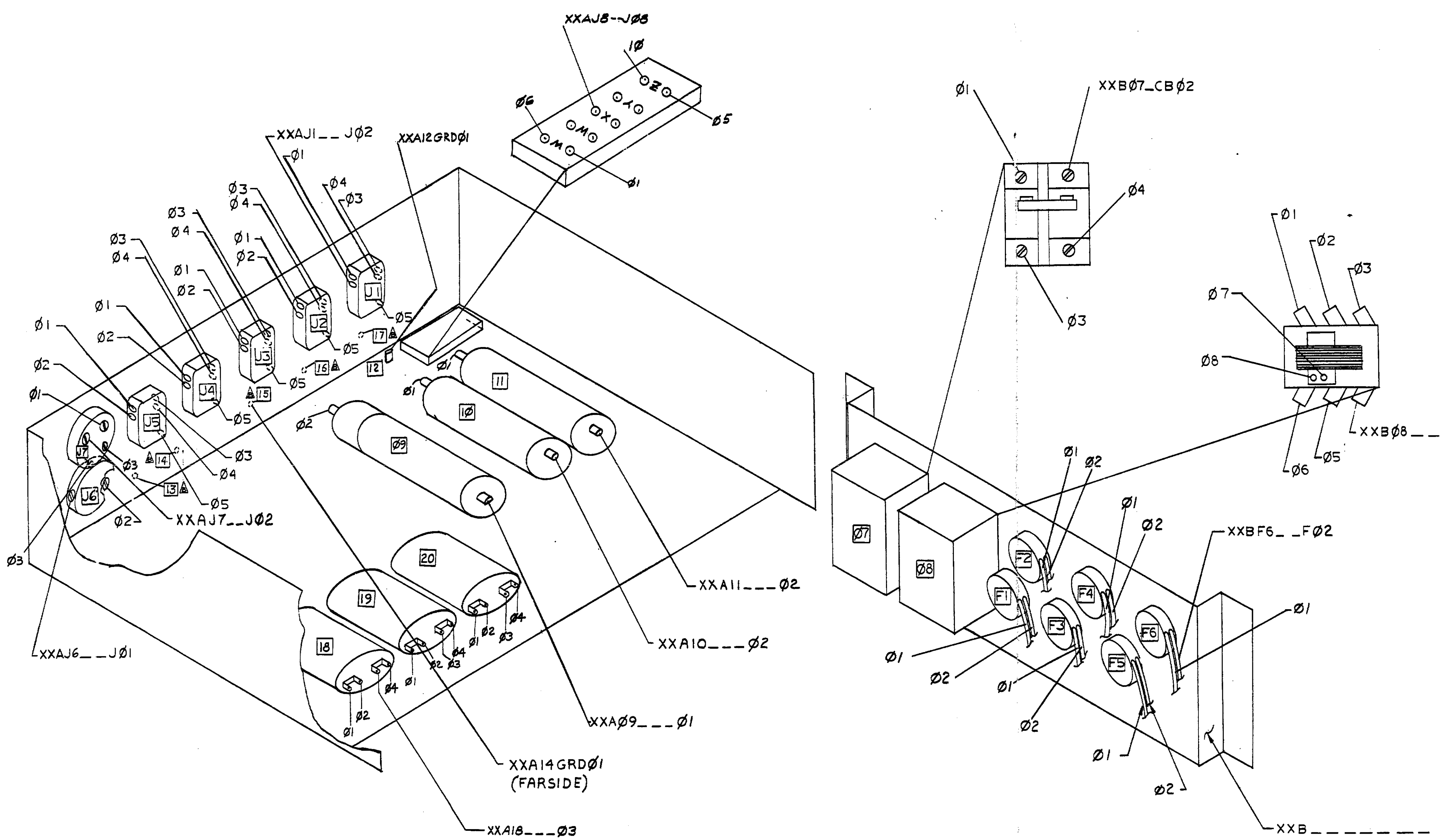
P70031961	PARTS LIST	
RECD 3 702	RECD 701	ITEM NO.	DRAWING NUMBER	DESCRIPTION	GOVT NO.

DR C.P. Murphy	8-6-71	HONEYWELL INC. COMPUTER CONTROL DIVISION OLD CONNECTICUT PATH, FRAMINGHAM, MASS.
CHK D. Fabbi FDR	8-20-71	
MGR APPD R.P. Dale	8-20-71	TITLE CHASSIS ASSY
MATERIAL		

900324-09	532.12
NEXT ASSY	USED ON
APPLICATION	

FINISH PER	CODE IDENT NO.	SIZE	DRAWING NUMBER	REV
PRIMARY	07573	D	70031961	G
SECONDARY				
FINAL	SCALE 1/2		SHEET 1 OF 1	

Figure A-4. Chassis Assembly (Ref. Drawing 70031961, Rev. G)



CHARACTER POSITION	DESIGNATION FUNCTION
1	FRAME
2	GROUP
3	ZONE
4,5	POSITION
6	LEVEL
7,8	COMPONENT
9,10	TERMINAL

Figure A-5. Coding Diagram (Ref. Drawing 70031976, Rev. D)

Cut Along Line

USERS' REMARKS FORM

TITLE:

DOC. PART NO. _____

DATED _____

ERRORS NOTED:

Fol

SUGGESTIONS FOR IMPROVEMENT:

Fo

DATE _____

FROM: NAME _____

COMPANY _____ M/S _____

TITLE _____

ADDRESS _____

_____ ZIP _____

HONEYWELL INFORMATION SYSTEMS INC.
CEOB
300 CONCORD ROAD
BILLERICA, MA. 01821
ATTN: CEOB PUBLICATIONS, MS 872-A

Honeywell

The Other Computer Company:

Honeywell

HONEYWELL INFORMATION SYSTEMS

Printed in U.S.A.

FT09, REV. Ø